Simulation Procedures for Successful Low Noise Amplifier (LNA) Design Using Discrete Components

By Sonoko Akamatsu, Scott Muir, and Larry Dunleavy

Guiding the user through the stages of a basic low noise amplifier design and optimization.

Introduction

This tutorial is intended to guide the user through the stages of a basic low noise amplifier design and optimization, with a goal of first-pass fabricated design success. This will be accomplished by providing the user with a project tutorial, starting with the design process and ending with a comparison between the software simulations and the model performances. This example used in this treatment is that of a low noise amplifier using a Modelithics-developed nonlinear model for an Avago ATF54143 PHEMT device along with Modelithics CLR models for all passive lumped components [1, 2]. The simulations shown were developed within Agilent Technologies' Advanced Design System (ADS) RF/Microwave circuit design simulation environment.

Design Process

In this design, a low noise amplifier application circuit was demonstrated at 1.9 GHz. As stated above, the design was started with a Modelithics nonlinear model for Avago ATF54143 PHEMT device and Modelithics CLR Models were used for all passive components. Figure 1 shows a systematic design process that can be followed with good success for cases where a reference design or application circuit is available from the vendor. The initial schematic described in this note was generated from the manufacturer application note [3]. Modelithics transistor and passive component models were then used as the basis for optimization of the performance, along with built-in ADS microstrip library models for distributed elements (MLIN, MTEE, etc.). Additional steps that can be followed to further improve this design flow would be to include electromagnetic co-simulation of the microstrip portion of the circuit and with volume manufacturability in mind to add a statistical Monte Carlo analysis including expected variability of the PCB board material properties and RLC component tolerances.

Basic Theory

The Noise Figure describes the signal-to-noise degradation due to a noisy microwave component. The Noise Figure is defined as the ratio of the total available noise power at the output of the amplifier to the available noise

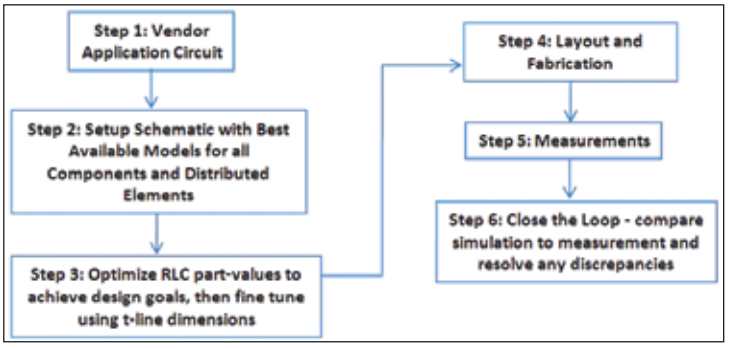


Figure 1 • Design flow followed for this example LNA design.

power at the input due to thermal noise from the input termination. The Noise Figure can be expressed as

$$F=\frac{SNRo}{SNRi}=\frac{P_{No}}{P_{Ni}G_A}$$

Where SNRi and SNRo are the signal to noise ratio at the input and output of the component and P_{No} is the total available power at the output of the amplifier, P_{Ni} is the available noise power due to the input termination and G_A is the Available Power Gain.

An alternate method for calculating the Noise Figure is expressed as

$$F = F_{min} + \frac{4r_n|\Gamma_s - \Gamma_{opt}|^2}{(1-|\Gamma_s|^2)|1+\Gamma_{opt}|^2}$$

F_{min}, r_n, and Γ_{opt} are known as noise parameters and are given by the manufacturer of the transistor or can be derived experimentally.

To achieve the minimum noise figure, $\Gamma_s = \Gamma_{opt}$ is chosen. However, simultaneous minimum noise figure and maximum gain cannot be obtained, in general. Therefore, the reflection coefficient, Γ_s can be selected that is a compromise between the Noise Figure and Gain performance [4]. The Available Gain can be calculated by

$$g_a = \frac{1-(|\Gamma_s|)^2}{1-(|S_{22}|)^2+(|\Gamma_s|)^2\cdot[(|S_{11}|)^2-(|\Delta|)^2]-2\mathrm{Re}(\Gamma_s\cdot C_1)}$$

$$G_a = (|S21|)^2\cdot g_a$$

Where $\Delta = S_{11}\cdot S_{22} - S_{12}\cdot S_{21}$ and $C_1 = S_{22} - S_{11}^*$.

Design Goals

Table 1 shows the design goals for this example LNA. The design approach and topology followed that determined by Avago Application Note 1222 as mentioned above. Series capacitors and parallel inductors were used for matching networks and a resistive loading method was chosen to maintain stability. Additionally source inductance was added to improve the input return loss. As a result, NF = 0.8 dB and Gain = 16 dB were obtained by an ADS simulation.

Parameter	Specification
Freq (GHz)	1.85-1.91
Gain (dB)	16
NF (dB)	0.8

Table 1 • Design Goals.

Device Simulation

Before proceeding to incorporate the application circuit topology and layout details, device simulation and stability analysis were performed on the transistor using the model. The S parameters and noise parameters were obtained from the Modelithics nonlinear model at the desired bias point and frequency. The results are shown in Table 2 and Table 3 under drain source voltage 3 V and gate voltage of 0.562 V. For this condition the simulated drain current from the model is 60 mA.

S11		S12		S21		S22	
Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.635	-178.602	0.066	31.124	7.759	72.566	0.188	-147.434

Table 2 • Model Generated S Parameter Results at 1.9 GHz (Vds = 3V, Vgs = 0.562V, Ids = 60 mA).

Fmin	0.45dB
Rn	2.785
Gamma opt	0.613<96.78deg

Table 3 • Noise Parameters at 1.9 GHz (Vds = 3V, Vgs = 0.562V, Ids = 60 mA).

The stability factor of the amplifier was simulated and also calculated by the obtained S-parameters [4]:

$$K = \frac{[1-(|S_{11}|)^2-(|S_{22}|)^2+(|\Delta|)^2]}{2\cdot|S_{12}\cdot S_{21}|}$$

For a two port network, unconditional stability is achieved when these criteria are satisfied: stability factor $K > 1$, and $|\Delta| > 1$. An alternate set of stability criteria is $K > 1$ and $b > 0$, with the b corresponding to the stability measurement given by:

$$b = 1+|S_{11}|^2 - |S_{22}|^2 - |S_{11}^*S_{22} - S_{12}^*S_{21}|^2$$

Figure 2 graphically shows that the transistor is potentially unstable at the design frequency band.

Manufacturer Application Circuit

An application circuit was designed based on the schematic and component parts list in Table 4 provided by the manufacturer [3]. Series capacitors and parallel inductors are used for matching networks. To ensure stability, resistive loads, 51 ohm and 10 ohm are used to improve input and output bias networks respectively as shown in Figure 3 below. The design of these bias networks are such that the effects of the 51 ohm input bias resistor are isolated from the RF part of the circuit by a 3.3 nH choke inductor and a 10 pF bypass capacitor, thus increasing the noise figure. A combination of 10pF and 10 nF were used for bypass capacitors.

In addition, source inductance was added for an improvement of input return loss. The measurement data of the manufacturer information indicates the potential for, 16 dB Gain at 1900 MHz, 0.7~0.8 dB Noise Figure from 1900 MHz through 2000 MHz, -6.4 dB Input Return Loss and -12.5 dB Output Return Loss under Vds = 3V at Id = 65mA.

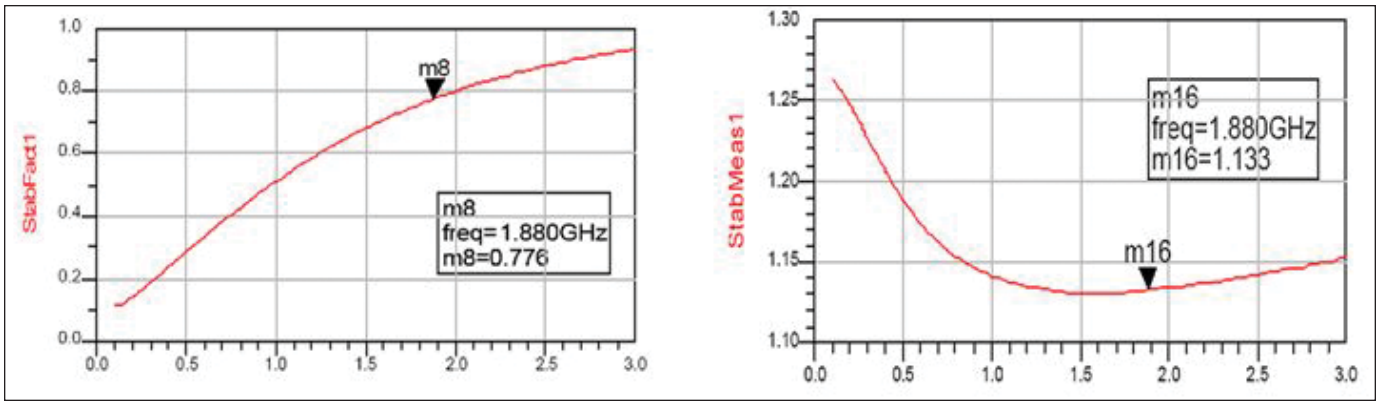


Figure 2 • Stability Factor (K) and Stability Meas (b).

Schematic Circuit and Optimization

Optimization is necessary to achieve the performance listed on the application note since the chosen substrate thickness and layout for this demonstration is different than that of the manufacturer's reference design [3]. In addition, details like the passive component size and manufacturer information are not listed in the application note. The available Modelithics models are tailored to the specifics of manufacturer component family and body style and are substrate scalable. Model inputs were setup for applicability to the 16 mil Rogers 4003 board chosen for this design. Figure 3 shows the schematic after optimization.

Figure 4 and Figure 5 include plots of the optimized simulation results. Simulations show a Gain of 15.8 dB at 1880 MHz, 0.7 dB Noise Figure, -5.4 dB Input Return Loss and -15.8 dB Output Return Loss under Vds=3V at Id=55.7mA. This is close to the manufacturer's performance [3]. Table 5 shows the updated optimized component part list using Modelithics Models.

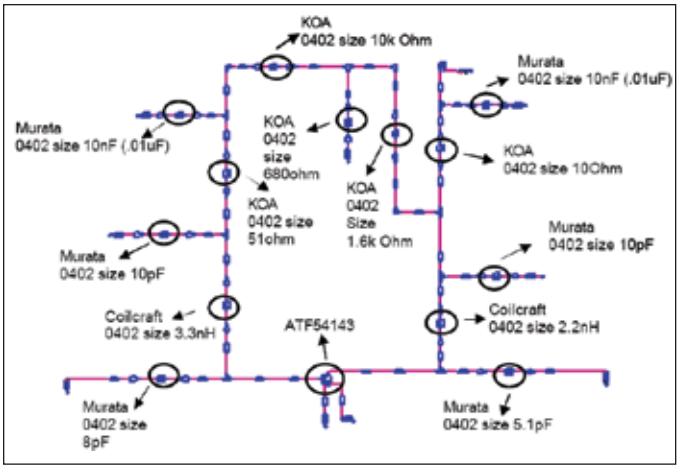


Figure 3 • Optimized Schematic for LNA. Models shown are Modelithics CLR passive models.

Layout and Fabrication

As mentioned above, a 16mil Rogers 4003 substrate was used for the board fabrication. RF probe pads and grounding pads were added into Figure 6 to facilitate testing with ground-signal-ground (GSG) RF wafer

	Item	Purpose
Q1	Agilent Technologies ATF54143 PHEMT	Transistor
C1	8.2pF chip capacitor	Input MN
L1	2.7nH inductor	Input MN & RF Choke
C2	8.2pF chip capacitor	bypass capacitor for high frequency
C3	10,000 pF chip capacitor	bypass capacitor for low frequency
R4	50ohm chip resistor	low frequency stability
C4	8.2pF chip capacitor	Output MN
L4	5.6nH inductor	Output MN & RF Choke
C5	8.2pF chip capacitor	bypass capacitor for high frequency
C6	10,000 pF chip capacitor	bypass capacitor for low frequency
R3	10ohm chip resistor	Stability
R1	300ohm chip resistor	Voltage Divider
R2	1200ohm chip resistor	Voltage Divider
R5	10kOhm chip resistor	Provide Current Limit
L2	Source Inductance	Improve Input Return Loss
L3	Source Inductance	Improve Input Return Loss

Table 4 • Manufacturer's Component Parts List for LNA Reference Design.

	Vendor Specified Item	As Optimized	Purpose
Q1	Agilent Technologies ATF54143 PHEMT		Transistor
C1	8.2pF chip capacitor	8.0pF chip capacitor	Input MN
L1	2.7nH inductor	3.3nH inductor	Input MN & RF Choke
C2	8.2pF chip capacitor	10pF chip capacitor	bypass capacitor for high frequency
C3	10,000 pF chip capacitor	10 nF chip capacitor	bypass capacitor for low frequency
R4	50ohm chip resistor	51ohm chip resistor	low frequency stability
C4	8.2pF chip capacitor	5.1pF chip capacitor	Output MN
L4	5.6nH inductor	2.2nH inductor	Output MN & RF Choke
C5	8.2pF chip capacitor	10pF chip capacitor	bypass capacitor for high frequency
C6	10,000 pF chip capacitor	10,000 pF chip capacitor	bypass capacitor for low frequency
R3	10ohm chip resistor	10ohm chip resistor	Stability
R1	300ohm chip resistor	680ohm chip resistor	Voltage Divider
R2	1200ohm chip resistor	1600ohm chip resistor	Voltage Divider
R5	10kOhm chip resistor	10kOhm chip resistor	Provide Current Limit
L2	Source Inductance	Source Inductance	Improve Input Return Loss
L3	Source Inductance	Source Inductance	Improve Input Return Loss

Table 5 • Manufacturer's Component Parts List Along with Modifications to Optimization using Modelithics Models (See Fig. 5 for details of usage in circuit).

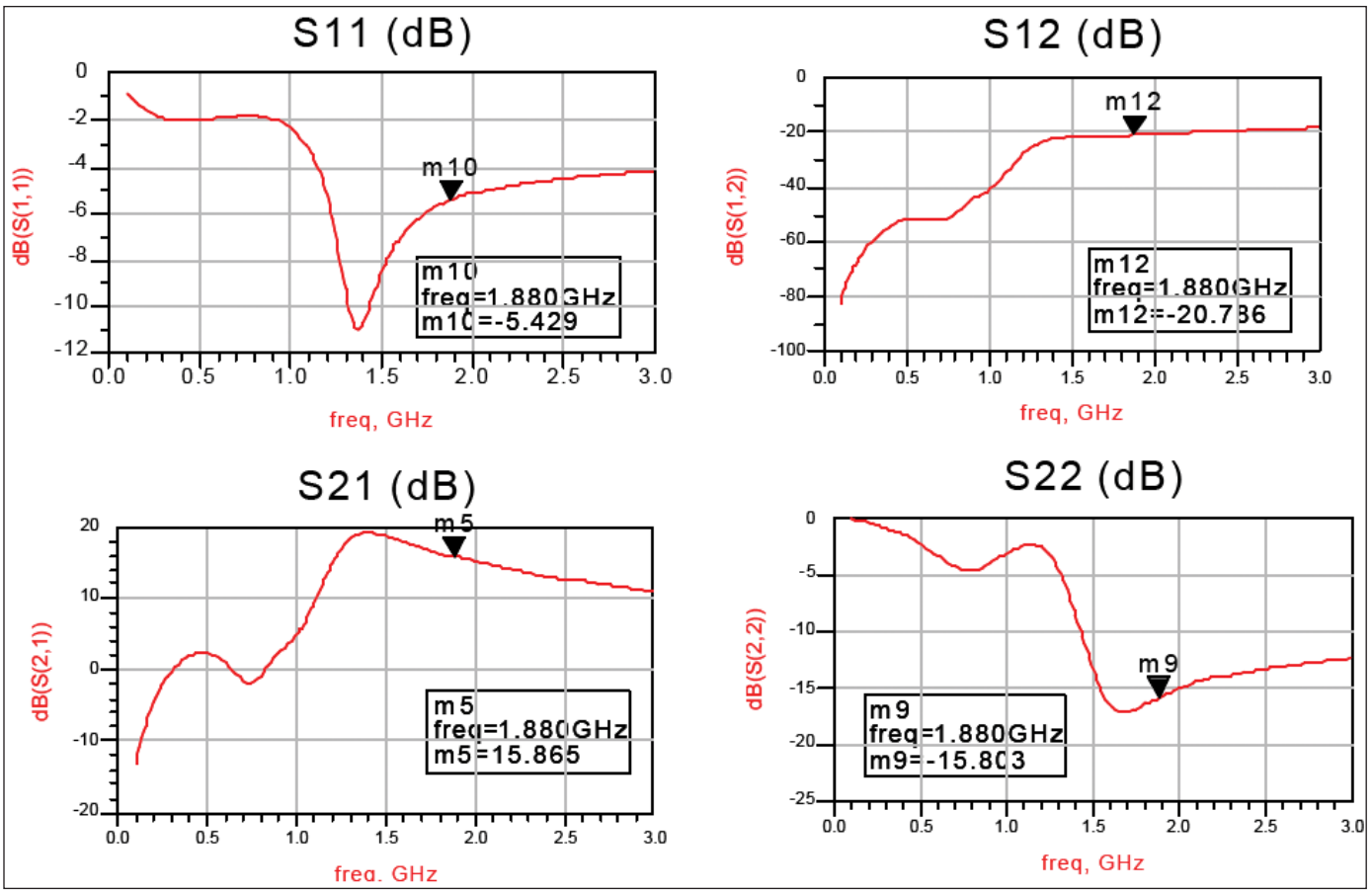


Figure 4 • Optimized LNA S-parameter Simulation Results. Vds = 3 V, Vgs = 0.562 V, Id = 60 mA.

probes. Figure 7 shows the complete assembled board. The board size is approximately 24mm x 18mm.

Comparison to Measurements

An Anritsu 37397C Vector Network Analyzer (VNA), J-Micro Wafer Probing Station and GGB 650 pitch probes were used for the measurements. A Thru Reflect Line (TRL) calibration was performed for these 2 port measurements using custom calibration standards fabricated on the same boards used for measurement. The results in Figure 8 show 17 dB Gain was obtained at 1.88 GHz when the amplifier was tested at a bias point of Vds=3V at Id=82mA. (Note that the transistor bias current is slightly different than that simulated due to transistor fabrication differences. Vds and Vgs values equal the simulated values, however the fabricated device uses a higher current.) Figure 8 also shows the comparison between simulation and measurement. The result shows the amplifier design achieved first-pass success. It should be mentioned that bench tuning or tweaking was done on this design after assembly. Figure 9 illustrates that the out-of band performance is also well predicted through 10 GHz. A comparison with measured Noise Figure is shown in Figure 10. These results show that simulation with Modelithics models agrees well with measurement data and verifies the success of the proposed design flow.

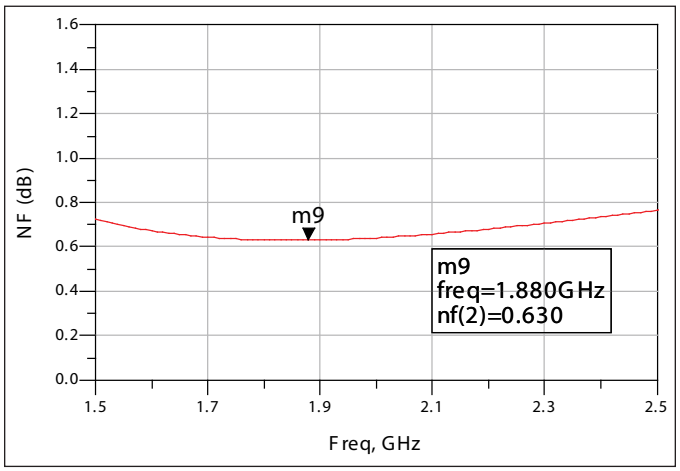


Figure 5 • Optimized LNA Noise Simulation Result. Vds = 3 V, Vgs = 0.562 V, Id = 60 mA.

To briefly explore alternative model results, Figure 11 includes a comparison between results achieved with Modelithics models, compared to that achieved with alternately available models. This included an alternative

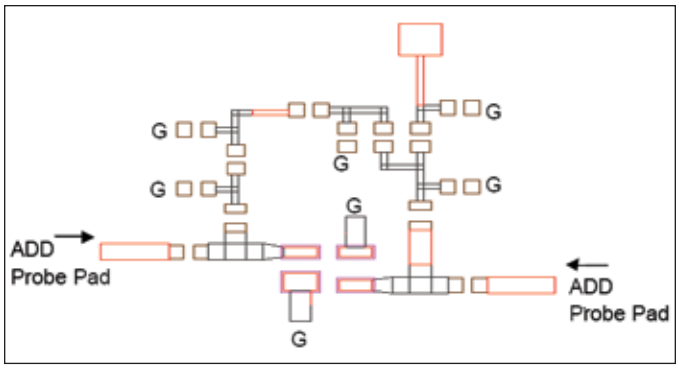


Figure 6 • LNA Layout.

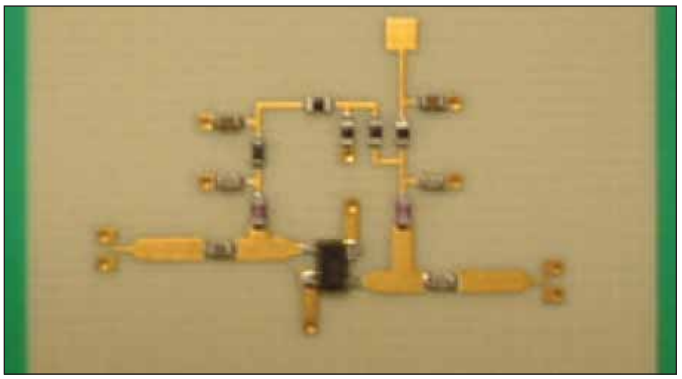


Figure 7 • LNA Assembled Board.

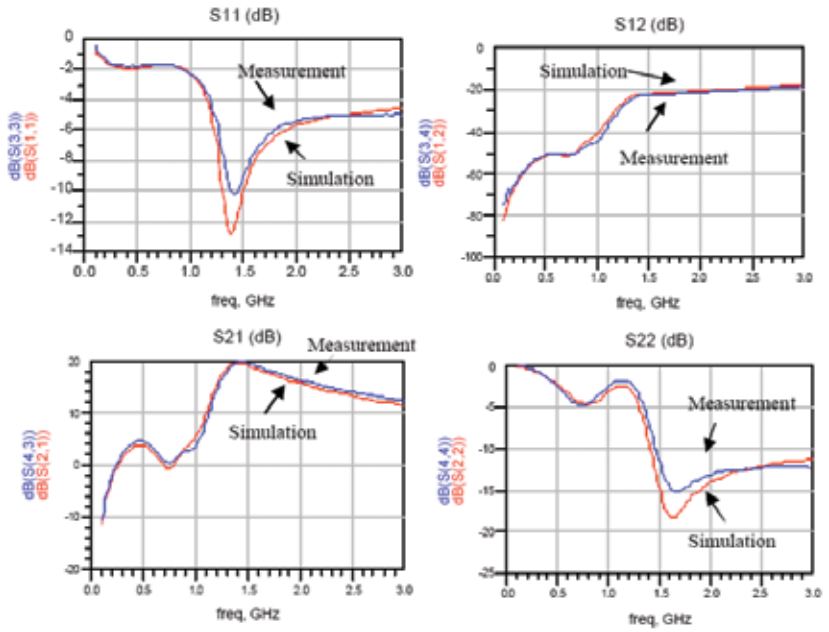


Figure 8 • Comparison of Measured (blue) and Simulated (Red). Bias conditions: Vds = 3V, Id = 82mA through 3 GHz.

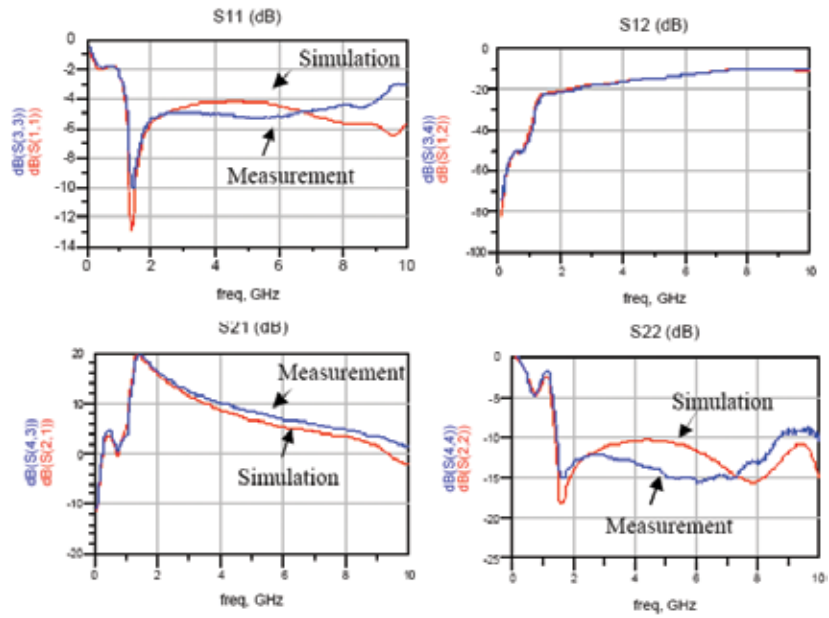


Figure 9 • Comparison Results for LNA Extended through 10 GHz at 3V, 82mA.

ADS Curtice model for the transistor available from the manufacturer's website along with both Modelithics Global Models and ideal passive models.

Summary and Conclusions

In this note, a 1.9 GHz Low Noise Amplifier application circuit was described that demonstrated a first pass success design approach. Avago ATF 54143 PHEMT device was chosen to satisfy the low noise requirement. The design flow started from the manufacturer application note and was optimized using a Modelithics model for the transistor and substrate-scalable Modelithics Global Models for the RLC components. A key feature of achieving first pass success with this design flow is the ability to account accurately for vendor specific performance and substrate effects of the passive models while being able to optimize the part values chosen to achieve the desired performance.

About the Authors:

Sonoko Akamatsu was a student intern at Modelithics, Inc. when this work was performed; she is now a Senior RF Design Engineer at TriQuint Semiconductor's New England Design Center, Chelmsford, Mass.

Scott Muir is an Electrical Engineering Intern at Modelithics, Inc., Tampa, Fla.

Larry Dunleavy is President and CEO of Modelithics, Inc., Tampa, Fla. He is also a Professor at the University of South Florida.

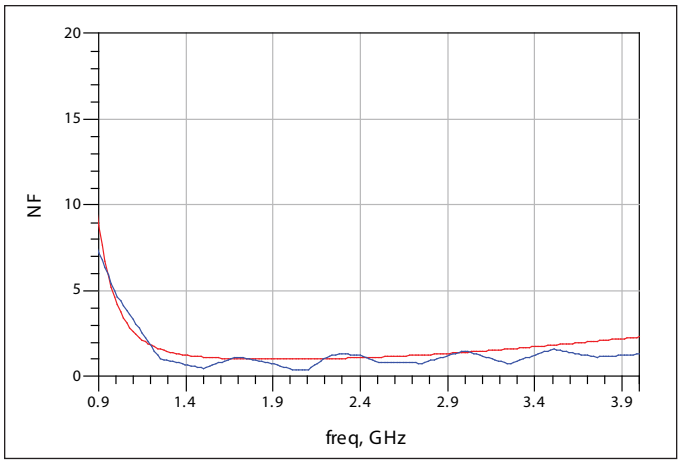
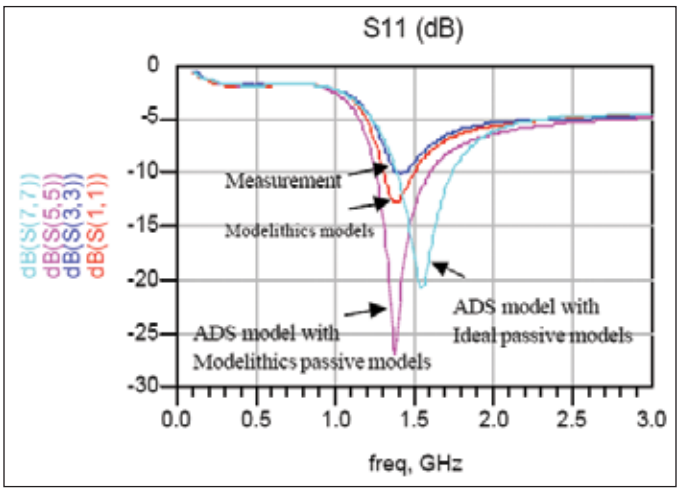
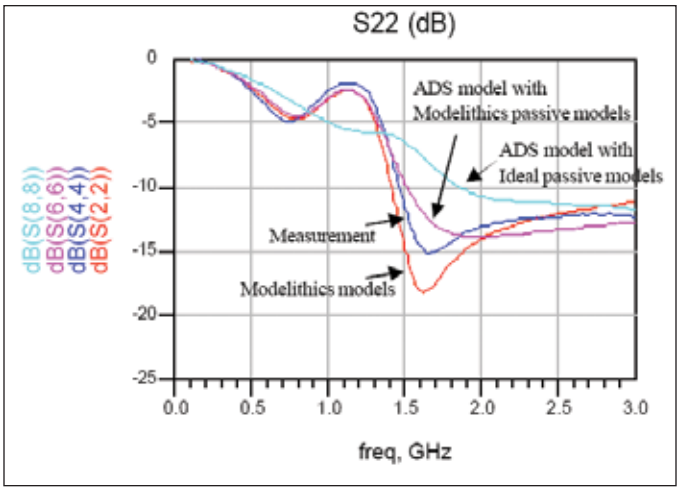


Figure 10 • Noise figure through 3.9 GHz. Red line – simulation, Blue line – measurement. Vds = 3V, Vgs = 0.562V, Ids=82mA.





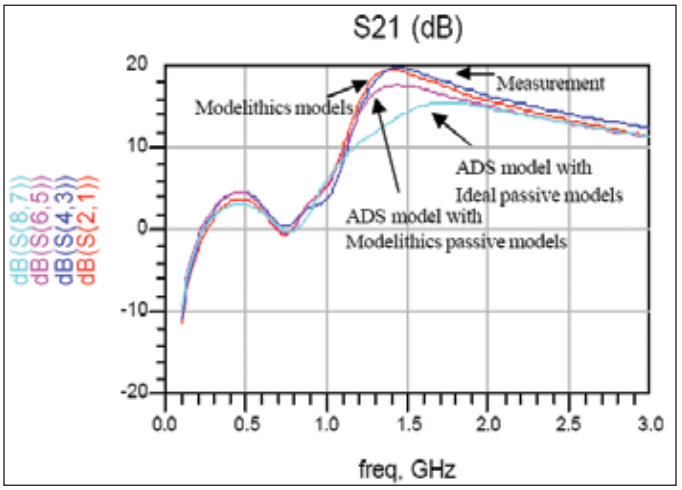


Figure 11 • Comparison of results, including Vendor S-Parameter Models for passives and available "ADS Model" and Modelithics models.

References:

[1] "Comprehensive Models for RLC Components to Accelerate PCB Designs," Microwave Journal, May 2004.

[2] Sonoko Akamatsu, "Application of Accurate Component Models for Improved First-Pass Microwave Circuit Design Success," MS Project University of South Florida, July 2005.

[3] Avago Technologies, "High Intercept Low Noise Amplifier for the 1850–1910 MHz PCS Band using the Enhancement Mode PHEMT", May 2010.
http://www.avagotech.com/docs/5989-2273EN

[4] Guillermo Gonzalez, "Microwave Transistor Amplifiers: Analysis and Design, "
Second Edition. New Jersey: Prentice Hall, 1997.

Acknowledgements:

The authors would like to acknowledge the assistance of Chris Reul, who assisted with some of the measurements shown in this paper while interning at Modelithics. Chris is now with Honeywell Company in Clearwater, Fla. We would also like to thank Rich Carlson and Laura Levesque for editing suggestions.

Contact information:

Modelithics, Inc., 3650 Spectrum Blvd., Suite 170, Tampa, FL 33612 • voice 888- 359-6539 • email sales@modelithics.com • web www.modelithics.com