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Design of Input Matching Networks for Class-E RF Power Amplifiers

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Class-E power amplifer design usually emphasizes output network design, but this article examines amplifier performance when an untuned input is replaced with a matching network

Class-E power amplifiers have high efficiency, which makes them attractive in modern wireless mobile communication systems. There are several techniques and approaches developed solely to design the output load networks of such amplifiers to shape the RF power device's output voltage and current for minimum power loss. However, little attention is brought to the design of the input matching network and to the device bias conditions, with their effects on the overall circuit performance. This paper attempts to discuss these topics through a systematic design and simulation approach for a typical 5 watt class-E power amplifier operating at 150 MHz.

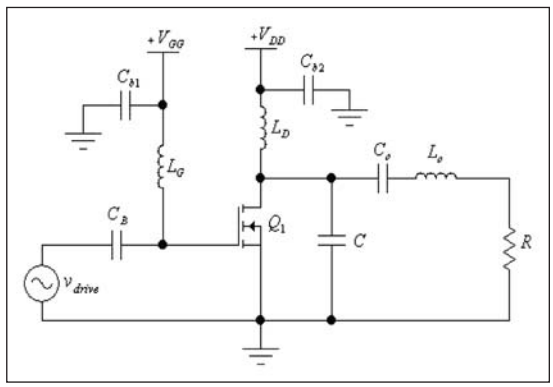

Figure 1 · Typical class-E power amplifier with shunt capacitance configuration.

Introduction

Several methods have been developed for the design of the load network for class-E RF power amplifier. Among those are the shunt capacitance [1], shunt inductance [2], finite DC feed inductance [3], and parallel circuit [4] techniques. The most popular configuration is the shunt capacitance technique due to its simplicity and *designability*, which means that when the amplifier is built as designed, it works as expected [1].

The schematic diagram of the class-E power amplifier with shunt capacitance configuration is presented in Figure 1. In this circuit L_G and L_D represent the gate and drain bias RF chokes respectively, C_B is a DC blocking capacitor, C_{b1} and C_{b2} are bypass capacitors, V_{GG} is the gate bias voltage, V_{DD} is the drain supply voltage, C is the capacitor shunting the active device Q_1, L_o and C_o constitute a series resonant circuit tuned at the operating frequency, and R is the optimum resistance seen by the load network for the required output power. The active device Q_1 (power MOSFET in this case) operates as an ON/OFF switch.

In class-E power amplifier circuit, efficiency is maximized by minimizing power dissipation in the active device, while providing the desired output power. The circuit can be arranged so that high drain voltage and high drain current don't exist at the same time.

For idealized class-E power amplifier operation, it is necessary to provide the following optimum conditions for the drain voltage $v_D(t)$ across the power MOSFET just prior to the start of the device's ON state at the moment $t = T$, where T is the period of the input driving signal [5]:

$$V_D(t)\big|_{t=T} = 0 \quad (1)$$

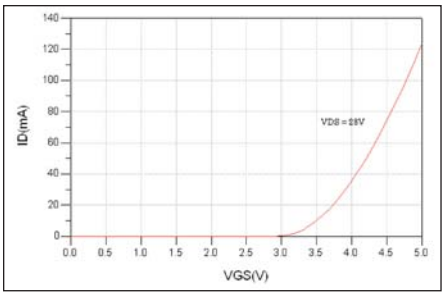

Figure 2 · I_D versus V_{GS} for the MRF134 power MOSFET.

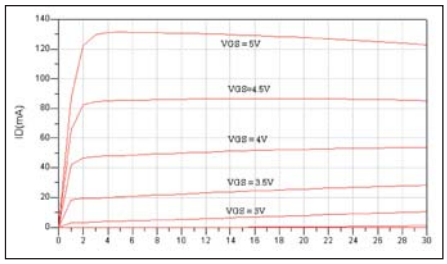

Figure 3 · Simulated drain DC characteristics of the MRF134 power MOSFET.

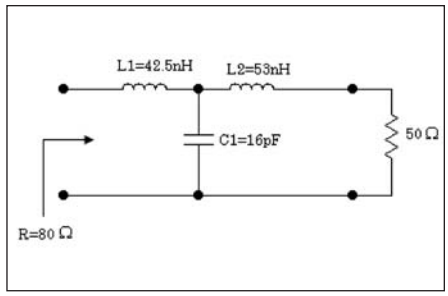

Figure 4 · Configuration of the output matching network.

$$\left.\frac{dv_D(t)}{dt}\right|_{t=T} = 0 \tag{2}$$

Equations (1) and (2) state that the drain voltage should be zero at the turn-on moment, and that the slope of this waveform is zero at the same moment.

Load Network Design Equations

The load network of class-E power amplifier is not intended to provide a conjugate match to the transistor output impedance. Design equations for the load network elements (C, C_0, L_0, and R) can be derived by writing time domain equations for the voltage $v_D(t)$ at the drain of the RF power MOSFET when it is OFF, and the current $i_D(t)$ passing through the RF device when it is ON. A set of simultaneous differential equations can be formed according to the necessary conditions (1) and (2) and solved to determine the network elements [6].

Nathan Sokal, the inventor of this amplifier, has developed explicit form equations to calculate the values of the network elements at any output power and loaded quality factor Q_L.

These equations are formulated as [7]:

$$R = 0.5768\left(\frac{V_{DD}^{\ 2}}{P_{out}}\right)\cdot\left(1-\frac{0.451759}{Q_L}-\frac{0.402444}{Q_L^{\ 2}}\right) \tag{3}$$

$$C = \frac{1}{5.44658\omega R}\left(1+\frac{0.91424}{Q_L}-\frac{1.03175}{Q_L^{\ 2}}\right)+\frac{0.6}{\omega^2.L_D} \tag{4}$$

$$C_o = \frac{1}{\omega R}\left(\frac{1}{Q_L-0.104823}\right)\left(1+\frac{1.01468}{Q_L-1.7879}\right)-\frac{0.2}{\omega^2 L_D} \tag{5}$$

$$L_o = \frac{Q_L.R}{\omega} \tag{6}$$

where P_{out} is the required output power, and ω is the operating frequency.

The value of Q_L can be selected based on a trade-off between operating bandwidth and harmonic distortion of the output signal.

Typical Class-E Power Amplifier Design

For the clarification of the goals of this paper, a power amplifier circuit has been designed and simulated using a commercial microwave CAD program. Design specifications of the amplifier are to achieve an output RF power of 5 W from an input driving level of 0.5 W, and drain efficiency of more than 65% at an operating frequency of 150 MHz.

The following sections describe a step-by-step design procedure with the simulated results obtained from the Agilent's ADS microwave circuit analysis program.

RF Power Device Selection and Characterization

The first step of the amplifier design procedure is the selection of the RF power transistor. For this design, the Motorola's power MOSFET MRF134 has been chosen. This device is capable of delivering 5 W at 400 MHz with a typical power gain of more than 10 dB. It operates from a 28 VDC supply and has a typical drain-to-source breakdown voltage of 65 V. The RF transistor library of the computer program ADS contains a SPICE model for this transistor which simplifies the simulation process. The simulated input DC characteristic (I_D versus V_{GS}) of the power MOSFET is shown in Figure 2 with V_{DS} = 28 V. It can be shown from this curve that the gate threshold voltage $V_{GS(th)}$ = 3 V. On the other hand, Figure 3 presents the simulated output DC characteristic (I_D versus V_{DS}) at several gate voltages. The drain ON resistance $R_{D(on)}$ can be estimated from Figure 3 as 12.5 Ω. This relatively large value of $R_{D(on)}$ will cause a reduction in amplifier's efficiency due to the dissipated power at the drain during the ON period of the power device.

Calculation of the Load Network Elements

The design procedure begins by calculating the component values of the load network using equations (3) to (6). For output power P_{out} = 5 W, operating frequency f =

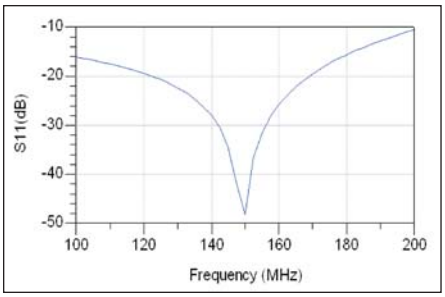

Figure 5 · Input return loss of the output matching network.

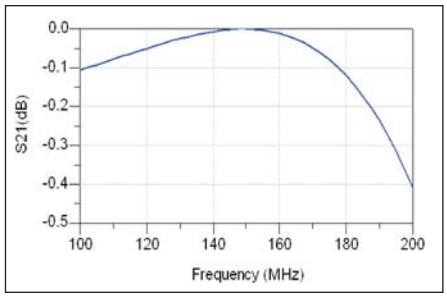

Figure 6 · Insertion loss of the output matching network.

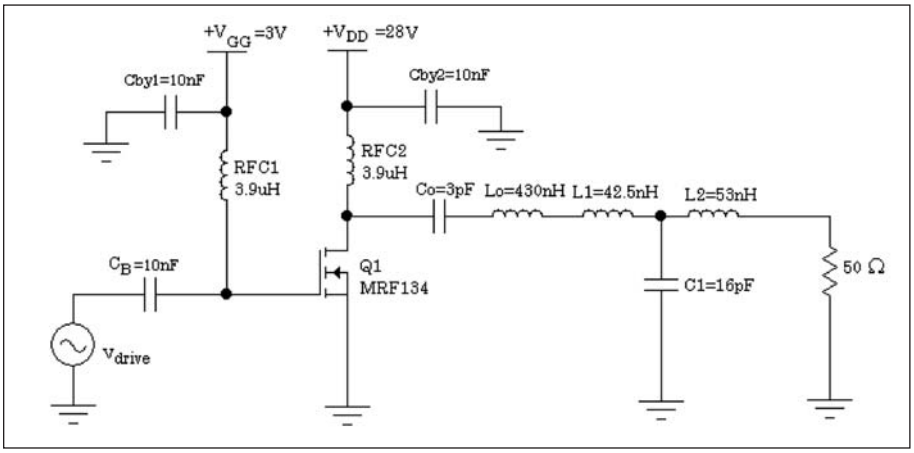

Figure 7 · The designed class-E power amplifier without the input matching network.

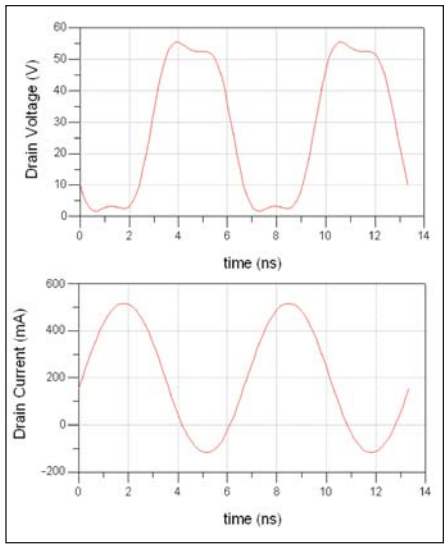

Figure 8 · Simulated drain voltage and current waveforms of the power MOSFET.

150 MHz, loaded quality factor Q_L = 5, and drain power supply V_{DD} = 28 V, the calculated values of the elements of the load network are:

R = 80 Ω, C = 3 pF, C_0 = 3 pF, and L_0 = 430 nH.

The output capacitance of the RF device, C_{out}, is measured as 9.7 pF from the device data sheet. This means that it is greater than the required value of the shunt capacitance. The excess value of 6.3 pF should be tuned out by part of the drain bias RF choke.

Design of the Output Matching Network

An output matching network is needed to transform the 50 Ω amplifier impedance into the required load resistance, which is set to be 80 Ω. This network has been designed with the aid of an immittance Smith chart, and is implemented in a T-section configuration, as shown in Figure 4.

In addition to the transformation function of the output matching network, it also can be used to reduce the harmonic content of the output RF signal. Figure 5 shows the simulated input return loss of this network, while Figure 6 presents its insertion loss versus frequency.

Design of the Biasing Network

The biasing network consists of the drain and gate RF chokes, bypass capacitors, DC blocking capacitors, in addition to the gate and drain bias voltages. For 50% duty cycle operation, the transistor is biased at the threshold point, which means that $V_{GG} = V_{GS(\text{th})}$ = 3 V. This bias point actually corresponds to class-B mode.

Based upon the previous calculations, the schematic diagram of the amplifier circuit is shown in Figure 7.

Amplifier Performance Simulation

The designed amplifier circuit has been simulated using ADS 2006A. With a single tone input signal of 0.5 W power level and an operating frequency of 150 MHz, the RF device's drain voltage and current are sketched as depicted in Figure 8. As shown from this plot, the peak values of drain voltage and current don't exist simultaneously which minimizes the device's power loss. However, at the ON time of the RF signal, the drain voltage is about 3.5V due to the ON resistance at the drain, $R_{D(\text{on})}$. This may degrade the overall efficiency of the circuit. During the OFF interval of the RF signal, a negative current flows through the power MOSFET's output capacitance C_{out}.

In Figure 9 the output signal waveform is plotted, while its spectrum is displayed in Figure 10. It is obvious that harmonics are reduced to acceptable levels due to the

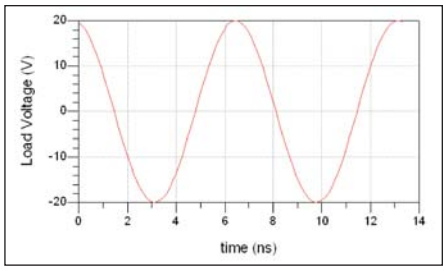

Figure 9 · Simulated waveform of the load voltage.

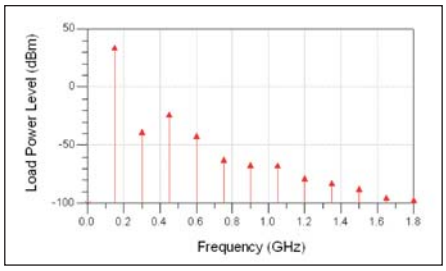

Figure 10 · Power spectrum of the output signal.

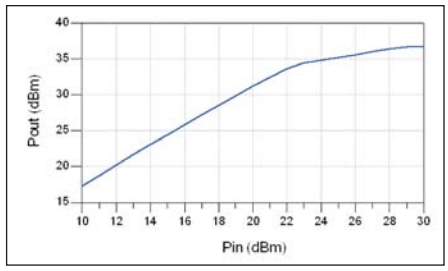

Figure 11 · Amplifier output power versus input power.

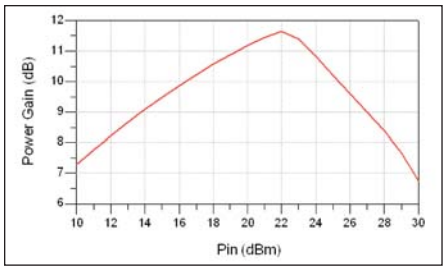

Figure 12 · Power gain versus input power.

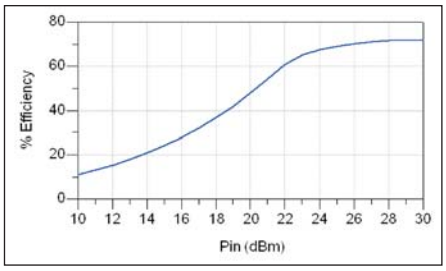

Figure 13 · Simulated efficiency versus input power.

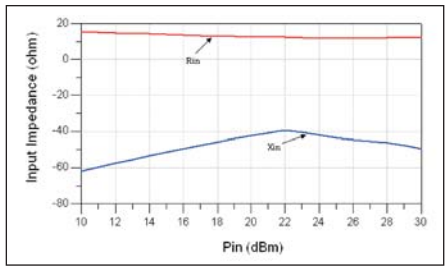

Figure 14 · Variation of the large signal MOSFET input impedance with input signal level.

filtering effect of the load and matching networks.

In order to display the power amplifier's performance characteristics, a sweep of the input power level has been carried out from 10 to 30 dBm at the operating frequency. Figure 11 shows a sketch of the output power versus input power. The output power is obtained from:

$$P_{out} = real\left(0.5V_L.I_L^*\right) \tag{7}$$

where V_L and I_L are the peak values of the fundamental components of load voltage and current respectively. The output power is about 36 dBm at an input level of 27 dBm.

Figure 12 presents the operating power gain of the amplifier, G_p, versus input power. The power gain is calculated from:

$$G_p(dB) = P_{out}(dBm) - P_{in}(dBm) \tag{8}$$

Notice that the power gain is about 9.0 dB at an input power level of 27 dBm.

Finally, Figure 13 displays a plot of the amplifier's DC to RF efficiency with input power. The amplifier efficiency is about 71.1% at an input power of 27 dBm.

The efficiency of the amplifier circuit has been evaluated from:

$$\eta = \frac{P_{out}}{P_{dc}} \tag{9}$$

where P_{dc} is the DC power consumed by the RF device and is obtained from:

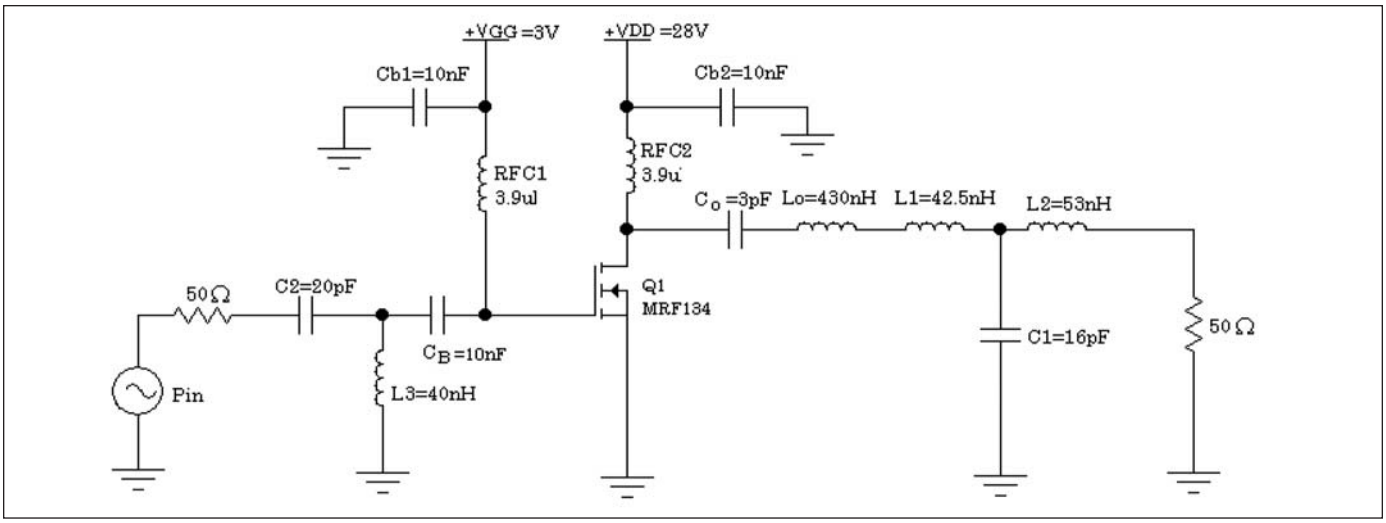

Figure 15 · The designed class E power amplifier after adding the input matching network.

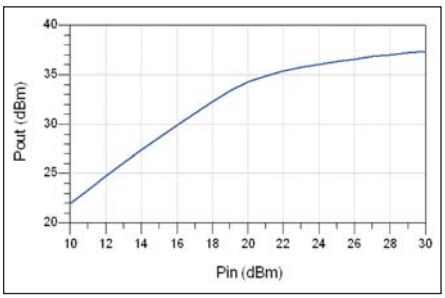

Figure 16 · The simulated output power versus input power for the final amplifier.

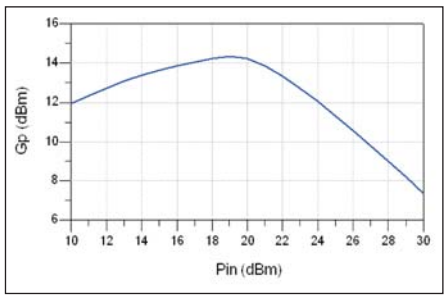

Figure 17 · Operating power gain versus input power.

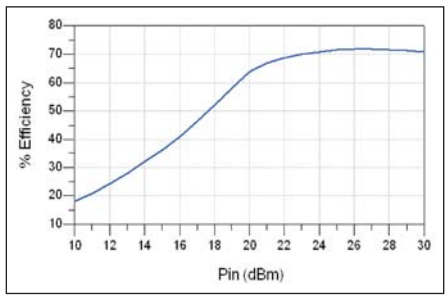

Figure 18 · Amplifier efficiency versus input power.

$$P_{dc} = V_{DD}.I_{DD} \tag{10}$$

where I_{DD} is the DC component of the drain current.

Input Matching Network Design

The input matching network can be designed to match the large signal input impedance of the RF power device with the 50 Ω source impedance. Therefore, the large signal input impedance of the RF transistor should be estimated at the nominal input power, operating frequency, and bias voltages with the existence of the load and output matching networks.

The large signal input impedance of the power transistor consists of two parts, resistance R_{in} and reactance X_{in}:

$$Z_{in} = R_{in} + jX_{in} \tag{11}$$

R_{in} and X_{in} can be estimated from:

$$R_{in} = real\left(V_{in} / I_{in}\right) \tag{12}$$

$$X_{in} = imag\left(V_{in} / I_{in}\right) \tag{13}$$

where V_{in} is the fundamental component of the input voltage at the gate of the MOSFET, and I_{in} is the fundamental component of the current entering the gate of the transistor. I_{in} can be estimated using a current probe with the aid of ADS simulation capabilities. Figure 14 shows a sketch of the large signal input impedance of the power device versus input power.

As shown from the plot in Figure 14, the input impedance is capacitive. At an input power of 27 dBm (0.5 W), the input impedance is approximately 12 $-j$45 Ω. The input matching network can thus be designed to match this value with the 50 Ω source impedance. An immittance Smith chart has been used to construct an L-section matching network graphically. Figure 15 presents the final power amplifier circuit after incorporating the input matching network.

There is no doubt that the input matching network improves the net input power delivered to the RF device. The amplifier circuit was simulated again after adding the input matching circuit using ADS. The output power of the circuit is displayed in Figure 16 with a sweep of input power from 10 to 30 dBm. As shown from Figure 16, there is a slight increase in output power being

38.8 dBm for an input power of 27 dBm. The power gain is plotted in Figure 17, and becomes equal to 9.8 dB at the nominal input power. The DC to RF efficiency is sketched in Figure 18 versus input power. The efficiency becomes 71.8% at an input power level of 27 dBm. However, no attempts have been made to optimize the component values of the input matching network for better performance characteristics.

Table 1 summarizes the performance of the amplifier before and after adding the input network.

	Before	After
Output Power	36 dBm	36.8 dBm
Power Gain	9.0 dB	9.8 dB
Efficiency	71.1%	71.8%
P_{in} = 0.5W (27 dBm), f_0 = 150 MHz		

Table 1 · Performance comparison before and after adding the input matching network.

Conclusion

The performance of Class E RF power amplifier with a traditional shunt capacitance load network has been studied thoroughly. It was shown that the high efficiency operation of such amplifiers is determined mainly by the output load network. However, with an accurate and proper design of the input matching network, the performance characteristics of the amplifier can be improved. This article has presented and discussed the main guidelines for synthesizing the input matching circuits for this type of RF amplifier to achieve the improved performance.

Acknowledgement

I would like to express my deep gratitude to Dr. Andrei Grebennikov for his continuous advice and useful suggestions in high efficiency power amplifier analysis, and also for providing me with some technical papers and e-books in the field of RF power amplifiers.

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