Mismatched Load Characterization for High-Power RF Amplifiers

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This article discusses the methods for dealing with RF amplifiers that operate into loads with impedances far from the typical 50 ohms, including many systems found in industry, science and medicine any applications for RF power amplifiers must deliver their power into loads with high Voltage Standing Wave Ratios (VSWRs). Among these applications are lasers, plasma chambers and ICP torches. It is impor-

tant to characterize the RFPA in order to understand its performance regarding stability, dissipation, efficiency, voltage breakdown, and power developed into mismatched loads.

This paper describes the techniques used to characterize an RFPA along with results obtained on a 45 MHz single transistor model. A multiple transistor RFPA at 80 MHz, used as a laser driver with a power output of 1200 watts peak, is also described. Protection methods are also discussed, and a follow up article will add information on matching circuits and components for high power matching. The information in this article applies primarily to saturated amplifiers operating in class C, D, or E and capable of efficiencies in excess of 70%.

45 MHz Test Amplifier

Figure 1 shows the schematic diagram of a 45 MHz final amplifier stage selected as a test model. This frequency was chosen because the transistor is capable of sustaining harmonics up to at least the fifth thereby generating a drain waveform consistent with a high-efficiency amplifier. The test results of the model are summarized below the schematic in Figure 1. [Figures begin on the next page.] The drain waveforms and frequency spectrum will be discussed later. The input and output circuits use

a two-step matching circuit to transform the low input and output impedances to 50 ohms. This matching method is better than a single step match because it's broader in bandwidth and the components are less critical. The gate voltage is used to switch the amplifier on and off when used in the pulsed mode as with a laser driver.

In order to gain insight into the mismatched performance of the amplifier, a model using a voltage generator in series with a source resistance (R_S) and a load impedance (Z_L) is shown in Figure 2. Figure 3 shows the manner in which the efficiency of an amplifier, simulated by the model, varies with the source resistance. The efficiency of an amplifier with a load resistance of 50 ohms and a source resistance of 20 ohms is about 72% and is used to represent the high-efficiency amplifier for analysis. While the model is quite simple, it gives remarkable insight into the characterization when compared with the actual test results. A more rigorous analysis would be a worthwhile project.

Figure 2 gives the equation for the series load impedance Z_L in terms of the reflection coefficient $\rho < 0$. Z_L can then be found for different VSWRs as the phase angle is varied around the Smith chart. From this the power developed (P_o) can then be calculated as shown by the equation. Figure 4 shows the manner in which the power varies for different source resistances for a VSWR of 2:1 ($\rho =$ 0.33). A constant voltage of 180 volts and a source resistance of 20 ohms are used for the calculations because, when used in the model, they result in a power output of 330 watts and an efficiency of 72%. This is close to the superpulse test results shown in Figure 1.

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Figure 1 · Schematic and data for the 45 MHz test amplifier final stage.

Notice how the developed power varies as the phase angle and source resistance are varied. For a 50-ohm source resistance, the power is flat versus the phase angle. As the source resistance is decreased, the power increases and is maximum at 0 = 180degrees. This is true provided the generator has a constant voltage and source resistance. For the assumed source resistance of 20 ohms, the power increases to 410 ohms where θ = 180 degrees and is greater than the 330 watts developed into a 50-ohm load. The characterization has been done for other VSWRs of 3:1, 4.9:1, and 9.5:1 and are discussed later.

In order to be able to compare the calculated characteristics with the test model of Figure 2, a test is conducted as shown in Figure 5. The test amplifier is operated in the pulsed mode at a pulse width of 200 µsec at a duty cycle of 10%. This enables the transistor to survive any mismatched condition without failure. Mismatches are placed ahead of the 50-ohm measuring system and the phase of



Figure 2 · Equivalent circuit model of source and mismatched load.

the mismatch varied using 15-degree lengths of coaxial cable. The power is measured using a peak reading power meter. The test results are shown in Figure 6.

Figures 7, 8, 9, 10 show how the calculated and measured data compare. It should be remembered in examining the curves, that a linear constant voltage generator was assumed along with a constant source resistance.



Figure 3 · Equivalent circuit model efficiency vs. $R_S(R_L = 50 \text{ ohms})$.



Figure 4 \cdot Calculated P_o vs. θ for $\rho = .33$ and $R_s = 50, 35, 20$ and 10 ohms.



Figure 5 · VSWR test arrangement.

The curves show that the tested amplifier follows the general shape of the calculated curves even though there is some error in the absolute values. The tested amplifier shows deviation from the calculated curve particularly for the 9.5:1 VSWR when the phase angle approaches 180 degrees. This is probably because the transistor cannot support the necessary current and the model no longer represents the transistor's operation.



Figure 7 \cdot P_o vs. θ , calculated and measured, VSWR = 2:1.



Figure 9 \cdot P_o vs. θ , calculated and measured, VSWR = 4.9:1.



Figure 6 \cdot 45 MHz test model VSWR performance; B+ = 48 V, pulse width = 200 µsec, duty cycle = 10%.

Transistor Drain Voltage Characteristics

The drain voltage waveforms of a transistor operating in one of the high efficiency classes of operation (C, D, or E) demonstrate voltages in excess of twice the B+ voltage. Figure 11 shows a photograph of the drain voltage of the



Figure 8 \cdot P_o vs. θ , calculated and measured, VSWR = 3:1.



Figure 10 \cdot P_o vs. θ , calculated and measured, VSWR = 9.5:1.

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Figure 11 · Drain voltage waveform into 50 ohm load.



Figure 12 · Frequency spectrum of Figure 11.



Figure 13 · Drain voltage waveform; operation into a 65:1 VSWR.

test amplifier into a 50-ohm load. The peak drain voltage is 160 volts, which is 3.33 times B+. Figure 12 shows a photograph of the frequency spectrum of the drain voltage connected to a Spectrum Analyzer using a capacitive probe where it is shown to support harmonics out to the seventh and beyond. Figure 13 is a photograph of the drain voltage when the amplifier is operated into a 65:1 VSWR at the phase angle that generates the maximum peak drain voltage. This voltage excursion is 200 V or about four times B+. When it is considered that the transistor is rated by the manufacturer at only 120 volts, the possibility of breakdown exists. Even so, transistors are consistently used in this manner. The peak drain voltage swing comes from energy stored in the resonant circuit after the transistor has turned off. It has been observed in transformer coupled push-pull pairs, that this peak drain voltage swing can be as much as 5 or 6 times B+ when the amplifier is operated into high VSWRs. The peak drain voltage swing comes from the opposite transistor as it turns on and comes from a different source than the single ended circuit in the test model.

In order for the amplifier to withstand these peak voltages without failure, a term 'Transient VSWR' perfor-



Figure 14 · Power output and power dissipated vs. θ for VSWR = 2:1; 45 MHz, 48 V, 200 µsec pulse width, 40% duty cycle, $R\theta$ = 0.6°C/W (MRF151).

mance has been coined. The VSWR test described previously is used to insure that the transistors are capable of withstanding this stress. It has been found that some manufacturers transistors are more rugged and will pass this test consistently while others are less reliable. There is no protection method that is fast enough to protect from this type of failure and transistor manufacturers do not specify their transistors to operate in this manner. The alternative would be to reduce the B+ to about 30 volts thereby reducing the peak power capability to 40%. This would be a major cost disadvantage and the Transient VSWR test has proven effective in producing reliable amplifiers without reducing the B+.

VSWR Power Dissipation Characterization

An amplifier's ability to operate reliably into a VSWR during its maximum average power output, is also part of the characterization procedure. The test procedure of Figure 5 is repeated into a VSWR of 2:1 at a duty cycle of 40% while reading the peak or average power as well as the DC current. The dissipation in the transistor can then be calculated and plotted on a graph as shown in Figure 14. Knowing the transistor's thermal resistance and the operating case temperature, it can be determined if the transistor is within reliable dissipation limits. A junction temperature of 140 degrees C is considered to be a safe margin. The maximum dissipation for this transistor is 150 watts with a heat sink that limits the case temperature to 50 degrees C.

Protection Methods

When the amplifier shown in Figure 1 exceeds the dissipation limit shown in Figure 14, a protection circuit must be activated to prevent possible failure. Figure 15 is a photograph of the detected output power for a pulse length of 200 µsec when the amplifier is operated into a 65:1 VSWR at a phase angle that causes maximum dissipation. The duty cycle is less than 10% so as not to be a factor. The droop in the detected output is caused by the transistor's junction heating. If the pulse were to be made



Figure 15 · Drain voltage waveform at 65:1 VSWR. A longer pulse would exceed thermal limits.

longer, the transistor could fail. The protection circuit must react quickly enough to prevent this from occurring. Two methods of protection have been developed and are discussed in the following sections.

The first protection method is used primarily for RF laser drivers. Protection in a laser driver must retain the full peak power instead of folding back the RF output other wise the laser will not strike. Lasers are usually difficult to strike when left off for a period of time and a pulsed format at full peak power acts like an automatic start-up circuit. Once the laser strikes and is correctly matched, the protection circuit is automatically disconnected. This method of protection limits the maximum pulse width and duty cycle when activated and is shown in Figure 16 for the CW case. The maximum pulse width is limited to 200 usec and the duty cycle is limited to 10%. Under these conditions, the transistors in the output stage can survive any VSWR at any phase angle of the reflection coefficient.

For this protection to be effective, the transistors must be free from selfoscillations between pulses.

In Figure 16, a VSWR comparator changes state when the reflected voltage exceeds the forward voltage at a predetermined VSWR set point. For the test amplifier described, this set point is for a VSWR of 2:1. The



Figure 16 · Basic pulse width and duty cycle limit VSWR protection.



Figure 17 · Basic foldback VSWR protection and feedback control.

output of the comparator is connected to AND gate A. The other input to AND gate A is connected to a 200 µsec one-shot generator. AND gate B is connected to the TTL input signal that is used to turn the RF generator on and off in accordance with the desired modulation of the laser. When a TTL signal is applied, the 200 µsec one-shot is activated and inhibits AND gate A from sampling the output of the VSWR comparator. At the end of the 200 µsec

pulse, the comparator's output can be sampled. If it's high, indicating that protection is needed, the output of AND gate A activates a 2 msec one-shot. This 2 msec one-shot in turn disconnects AND gate B from the bias that controls the gate voltage on the RF transistors. Should the comparator output remain low no protection is initiated.

The waveform for CW protection is shown as a 200 µsec pulse at a 10% duty cycle. For pulsed operation additional circuitry is required but is not covered here.

The second method of protection folds the RF output back in proportion to the magnitude of the VSWR. It is used for RF generators that excite plasma chambers or ICP torches. Referring to Figure 17, the output power of the RF generator is controlled by the B+ output of a switch-





Figure 18 · Block diagram of a 1200 watt peak power amplifier for laser driver applications.

ing regulator. A 0-10 volt control voltage is connected to the + input of operational amplifier A. The - input to the operational amplifier is connected to the output of operational amplifier B that samples the forward and reflected voltages from a directional coupler at its inputs. Operational amplifier C's + input is connected to the output from operational amplifier A. Its - input is connected to the forward output of the directional coupler. The output of operational amplifier C controls the reference voltage of the switching power supply and therefore the B+ voltage for the RF amplifiers. The forward voltage from the directional coupler is thereby compared with the 0-10 volt input and any error between the two is corrected by the amount of feedback. 20 dB of feedback will reduce the error by a factor of 10:1.

When the reflected voltage exceeds the set point forward voltage, the output of operational amplifier B connected to the - input of operational amplifier A begins to control the B+ output thereby folding back the power in accordance with the magnitude of the VSWR. The gain of the fold-back loop determines the steepness of the fold-back curve in the lower right of Figure 17. It needs to be steep enough so that the dissipation in the transistors is below the maximum allowed but no steeper than necessary in order to generate the maximum allowable mismatched power for the chamber or torch. The speed of response needs to be greater than 500 µsec in order to adequately protect the transistors.

A 1200 Watt Peak 80 MHz Laser Driver

Figure 18 is block diagram of a 1200-watt peak laser driver at a frequency of 80 MHz. Two push-pull pairs are combined at the output using broadband transformer combiners. Emphasis is placed on stable performance into high VSWRs since high power lasers have low losses in their resonant structure and can be difficult to strike and match. The laser can have a VSWR as high as 50:1 before striking and the RF driver must generate maximum voltage into this mismatch. Figure 19 shows the VSWR characterization curves for this laser driver. The laser and RF driver are integrated by rotating the laser's unlit reflection coefficient phase angle back to the RF laser driver to match the maximum generated power output shown by the curves. This angle is about +160 degrees and would require a 50-ohm cable 50 degrees long for best striking and pulsed characteristics if the unlit reflection coefficient of the laser is -100 degrees.

1400 1300 -1200 è 1100 2.4:1 1000 900 3.5:1 800 700 500 7.3:1 400 300 24: 100 -160 -140 -120 -100 -40 -20 0 20 40 60 100 120 140 160 Coefficie nt Phase Angle

Figure 19 · VSWR characterization curves for the amplifier of Figure 18.

Summary

This paper has demonstrated that high-efficiency amplifiers can be characterized for their ability to drive mismatched loads. Such characterization data is important for applications such as lasers, plasma chambers, ICP torches and others. The drain voltage excursions have been shown to be three to five times the B+ voltage under mismatched conditions and amplifiers need to be tested in order to prevent failures. Methods of testing and protection under mismatched conditions have been presented.

The characterization analysis was based on a simple voltage generator model to demonstrate the amplifier's mismatched performance, but a more rigorous investigation would be a worthwhile project.

Coming Next

In the next issue of this magazine, a follow-up article will discuss matching network design and components for high power matching.

Author Information

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