# Recent Developments in Signal Integrity Theory and Practice

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Signal Integrity is at the center of high speed digital design, as clock rates reach higher into the GHz ranges. At these frequencies, the physical structure of component packages, p.c. boards, cables, connectors and enclosures becomes large in terms of wavelength. Even "ground" is no longer constant, since signals can propagate along conductive surfaces.

Table 1 shows the major issues in signal integrity engineering. These challenges are being addressed by the engineering staffs of OEMs, as well as the vendors of EDA tools, test equipment, foundry services, and p.c. board or contract assembly services. A technical note from **Sigrity Inc.** (www.sigrity.com) sums up the issues like this:

"Timing is everything in a high-speed system. Signal timing depends on the delay caused by the physical length that the signal must propagate. It also depends on the shape of the waveform when the threshold is reached. Signal waveform distortions can be caused by different mechanisms. But there are three mostly concerned noise problems:

- Reflection Noise
  Due to impedance mismatch, stubs, vias and other interconnect discontinuities.
- Crosstalk Noise
  Due to electromagnetic coupling between signal traces and vias.
- Power/Ground Noise
  Due to parasitics of the power/ground delivery system during drivers' simultaneous switching output (SSO). It is sometimes also called Ground Bounce, Delta-I Noise or Simultaneous Switching Noise (SSN)."

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| **PC Board Design** |
| Traces as transmission lines |
| Termination not purely resistive |
| Layers and via holes create discontinuities |
| Ground plane far from ideal |
| Power distribution and filtering is important |
| Discontinuities create reflections |
| Full board analysis is very large EM problem |
| **Jitter and Other Timing Issues** |
| Small timing errors are magnified at GHz |
| **Measurement and Troubleshooting** |
| Probes interact with the circuit |
| Test equipment must have extreme bandwidth of 3× to 5× clock rate |
| **Simulation Issues** |
| Large Size of EM Problem: |
| *Multi-CPU techniques* |
| *Choice of boundary conditions* |
| *Behavioral models to simplify analysis* |
| Engineering Point of Reference: |
| *S-parameters* |
| *Y-matrix* |
| *End-to-end BER/Eye diagram* |
| *SPICE vs. EM vs. Circuit Simulation* |
| Defining "ground": |
| *Equivalent circuit (behavioral model)* |
| *Conductor grid (EM simulation)* |
| *L-C matrix (circuit simulation)* |
| Jitter Models |
| BER Evaluation Methods |

**Table 1 · Key issues in signal integrity engineering.**

While the interest of *High Frequency Electronics* readers is primarily the signal path, the issues of ground and power quality are critical, as pointed out in the white paper, "Understanding Grounding Concepts in EM Simulators," by Dr. John Dunn of **AWR** (www.awrcorp.com):

"Misunderstanding how ground is implemented in circuit simulation is one of the most common misuses of electromagnetic (EM) simulators and their results. ... ground is a concept that, while perhaps a bit elusive, forms an important basis for how transmission lines are modeled and simulated. Just as the notion of 'what is ground' and 'where is it' changes as the underlying physics are probed, so too when real circuits are being analyzed."

## Design, Measurement and Research Trends

Table 2 lists trends in current signal integrity work. Research activities are underway in all of these areas; the separate "research" category was included to highlight areas of fundamental research, as opposed to R&D efforts that are directed to specific issues. The remainder of this article reports on activities addressing topics on this list.

Addressing the issues of EDA tools for chip design, **Sigrity, Inc.**, a provider of signal and power integrity solutions, recently announced that the major IC foundry

**Design Trends**

Board Design:
- *Done by OEM or contract manufacturer*
- *Growing use of microwave-type EM tools*

Chip Design:
- *Different people at OEM*
- *Outside design houses*
- *Close collaboration with fabs*
- *Both standard and vendor-specific tools*
- *Interface between device and board*

**Performance Evaluation**

Eye Diagram:
- *System tools now used at board level*
- *Still has subjective aspect*
- *Can help locate source of a problem*

Bit-Error Rate (BER):
- *End-to-end system tool*
- *Not the best method to pinpoint cause of poor performance*
- *Requires the proper test signal*

Choice of Test Equipment:
- *High speed oscilloscopes*
- *BER testers*
- *Microwave network analyzers*
- *System-specific testers (PCI, DDR, etc.)*

**Research Trends**

Greater Precision for Key Physical Models:
- *Via holes*
- *Packages*
- *Interconnections*

Alternative Technologies:
- *On-chip optical interface*
- *Asynchronous "clockless" operation*

**Table 2 · Trends in signal integrity research.**

**TSMC** (www.tsmc.com) has included three Sigrity chip, package and system co-design products—XtractIM, OrbitIO Planner and OptimizePI—in its new TSMC Reference Flow 11.0. Companies that rely on TSMC flow support for their IC designs now can benefit from these tools, which provide streamlined IC package assessment, package model extraction, chip/system IO planning, and power delivery system optimization.

**Ansys** (www.ansys.com) offers the latest DesignerSI package, including the Ansoft Designer integrated schematic capture and layout graphical user interface (GUI), 2-D quasi-static field solver and the Nexxim circuit simulation technology (transient, fast convolution, statistical, and IBIS-AMI). DesignerRF includes the Ansoft Designer desktop, 3-D planar electromagnetic field solver, RF system simulation tool, design synthesis tools, circuit simulation, powered by Nexxim (linear and nonlinear frequency domain). The DesignerSI product suite supports engineers designing high-speed electronic interfaces including XAUI™, XFI, Serial ATA, PCI Express™, HDMI™, DDR, DDR2 and DDR3.

**Simberian Inc.** (www.simberian.com) conducts significant work into the development of accurate EM simulation models for structures that affect signal integrity. A recent presentation from the company analyzed the effects of coupling capacitors on signal integrity, noting, "Serial multi-gigabit data channels have capacitors that may be connected in series (AC coupling capacitors) to allow different DC supply for a driver and receiver. Mounting structures of such capacitor and capacitors themselves can be considered as discontinuities for high-frequency harmonics in the channel. The observable effect of such discontinuities depends on the capacitor behavior, geometry of capacitors mounting structure as well as on location in the channel." The note includes data acquired using the company's Simbeor EM tool.

A recent paper from **Computer Simulation Technology** (CST – www.cst.com), "Signal Integrity Analysis of a Complex Multi-Layered Package," notes the importance of DC power distribution, ground and via holes. The paper demonstrates the simulation tools and setup methods that result in good agreement between simulation and measurements from a few MHz to 6 GHz, for a multi-layer IC package.

Research in signal integrity is an active area of study at **Penn State Harrisburg** (www.psu.edu). An example is provided by a 2005 paper comparing de-embedding methods, which are essential for high frequency/high speed measurements. Some test fixtures cannot be measured directly, therefore, efficient de-embedding techniques that heavily rely on simulation are used to characterize these fixtures. The de-embedded results of *S*-parameter and Fourier Transform based approaches were found to be similar, however, the Fourier transform produces a discrepancy in the step response, likely due to the loss of phase information when using this method. The authors found the two methods simple to implement, providing promising results.

Another paper from this school analyzed via hole modeling for the well-known microwave EDA tool, Advanced Design System (ADS) from **Agilent Technologies** (www.agilent.com), aided by the EM tool HFSS from **Ansys**. An extraction technique was used to develop an equivalent circuit model for an entire circuit structure, which was validated by comparing the results of HFSS with the equivalent circuit simulation. The goal of the research was to develop a circuit-based model that includes the effects of the via holes, which would allow much faster simulation of the entire system.

## Summary

Signal Integrity is an essential part of both product R&D and basic research for high speed digital circuits. The necessity for maintaining high quality signal transmission from chip to package, and from package pins across p.c. boards to other devices, is driving extensive study of computer simulation as well as measurement techniques for real signals. These methods, in turn, are used to create robust designs that sufficiently reduce the problems of waveform shape and timing, allowing reliable, error-free transfer of high speed data.