Probe Testing of Wafer Level Chip Scale Packaging

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Eliminating the"probe tower" in automated wafer probe systems reduces the size and complexity of the test system, improves test accuracy, but requires more precise mechanical interface tolerances

Wafer Level Chip Scale Packaging (WLCSP) has enabled smaller and thinner semiconductor devices with greater functionality to be used in consumer mobile applications such as smart phones, tablets and hand held GPS tracking devices. There is an accelerating trend toward wafer level chip scale packaging, with estimates placing growth at 26% CAGR for 2011 (Yole Marketing, 2011). WLCSP has lead the way to reduced cost of complex semiconductor devices through simplified packaging and a reduction in the number of touches in the semiconductor test process. Paradoxically, simplified WLCSP packaging demands have increased the demands on the test cell, including the test system, wafer prober and the interface to the device under test.

One of the more significant impacts is the signal performance requirements that were required at final package test are now shifted to the wafer probe environment, where pad-to-pad and ball-to-ball dimensions and tolerances are much smaller than those at final test and continue to shrink. This is most clearly seen in the device contacting requirements. At final test of a packaged device, alignment of the device under test (DUT) to its test socket and contacts is independent of the number of parallel test sites (multi-site test), and each

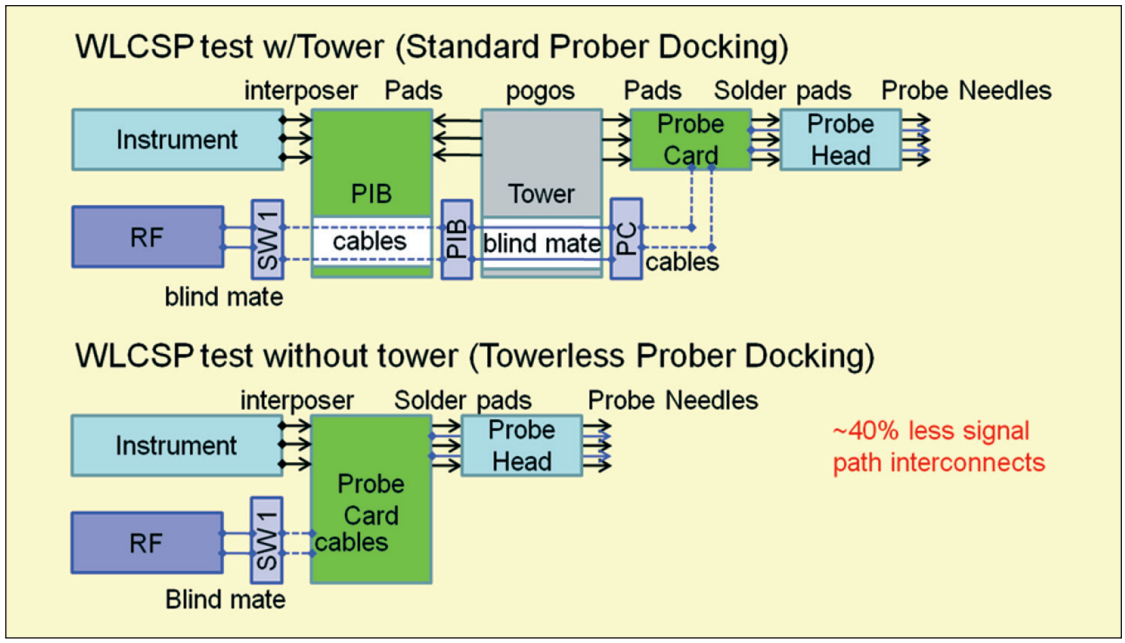

Figure 1 · Comparison of test procedures with, and without, a probe tower.

test site has alignment features in the socket that positions the packaged device with respect to the contacts. With wafer chip scale packing parallel test sites are no longer physically decoupled because they are all on the common wafer. Planarity and alignment errors become cumulative.

Multi-site test is essential to obtaining optimal test economics. While multi-site probe has long been a solution for testing pure digital and memory devices, complex analog and mixed-signal SOC devices add complexity to test floor management because these devices tend to be of lower volume and a greater variety. This leads to a higher frequency of reconfiguring the test cell to accommodate the changing mix of device types. In order to obtain the efficiencies of multi-site test in the face of these challenges it is important to focus on these essential requirements of the test cell:

1. Provide for minimal signal path from instrument to DUT.
2. Provide highly accurate and repeatable planarity alignment to support the requirements of membrane and fine-pitch, high-performance probe technology.
3. Provide for rapid changeover and setup of probe cards to minimize down time in high mix, low volume production environments.

It has been demonstrated that test cells can meet each of these requirements resulting in changeover of probe cards, performed by an operator in a production environment, meeting the required planarity, all in a matter of minutes. Let's consider each of these requirements.

Signal Path

In the past, wafer probe test interfaces have been based on the use of a probe tower to provide flexible solutions to meet low-to-medium performance requirements. These solutions consist of a probe interface board (PIB) that resides on the tester signal interface and a probe tower that extends test signals from the PIB into the prober to a probe card, which provides the needles to make contact with the wafer. These are lower cost solutions where only the probe card needs to be changed over to accommodate a different device. It also requires only reasonable mechanical accuracy for positioning the tester interface to the plane of the wafer. The layer of mechanical decoupling provided by the probe tower comes at the price of extending signal path length between the tester instrumentation to the probe needles and adding interconnects, both of which can degrade electrical signal performance due to impedance discontinuities.

Even though there is signal degradation, many analog signals can be addressed with calibration or error de-embedding techniques as is done with RF (radio frequency) signals. In comparison, digital signals can be sensitive to overall round-trip delay and are impacted by reflections at multiple interconnect boundaries. Reflections at high data rates lead to inter-symbol interference and data dependent jitter of signal edges. These effects are much more difficult or impossible to remove and can only be controlled by reducing the overall path length and eliminating interconnects. As high performance functional test moves to the probe environment and digital speeds continue to increase, the path effects become an unavoidable obstacle and a key limiter to signal performance. Towerless solutions minimize these effects and come closest to the original design intent of the tester's signal delivery system.

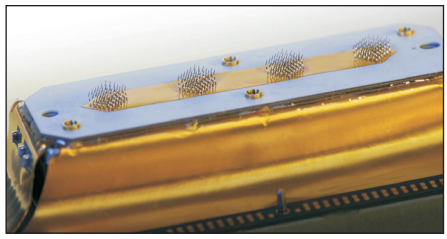

Figure 2 · Close-up photo of contacts on a test probe from Microprobe Inc.

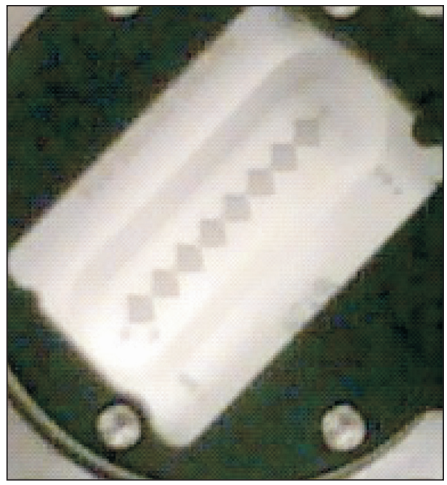

Figure 3 · Dies are accessed along a diagonal pattern.

Probe Technology	Planarity Requirement
Pogo Probes – Supplier A	0.090º
Pogo Probes – Supplier B	0.164º
Membrane Probes – Supplier C	
Max Allowable	0.057º
Recommended	0.029º
Measured Towerless planarity	0.029º

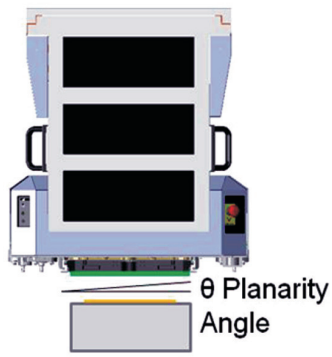

Figure 4 · Summary of planarity requirements for three types of probes.

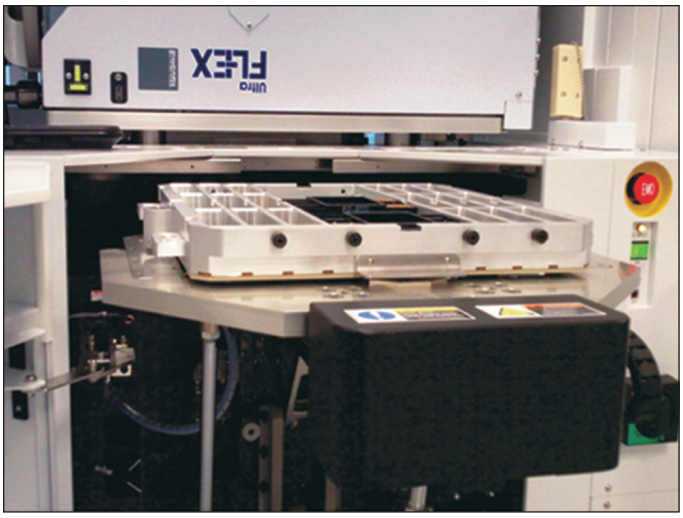

Figure 5 · Photo of the wafer probe system hardware.

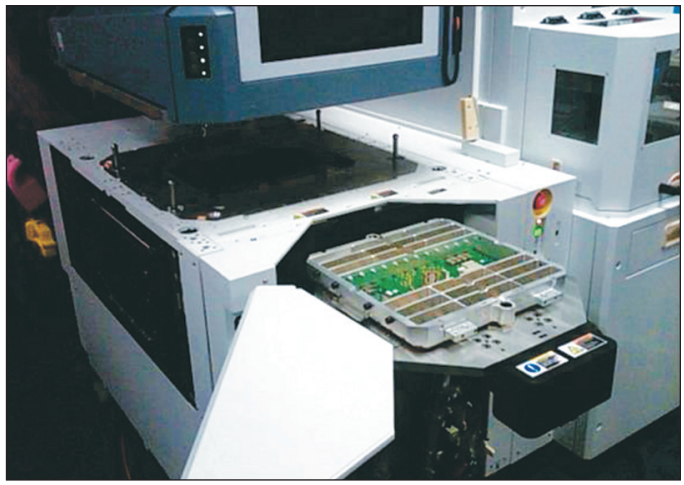

Figure 6 · This diagram illustrates the reduction in complexity of the new prober system.

Planarity

High performance function test wafer probe requires a solution that overcomes issues of interconnects and extended signal path lengths. For highest performance into the gigahertz region, membrane probes have proven to provide the best environment for controlling impedance to within 10s of µm of the die pad or solder ball. Other technologies such as pogo pins, cobra probes or buckling column probes also can maintain very short lengths to minimize inductance and achieve best performance. In all cases the *z*-axis compliance of these short probes is limited, requiring the probe interface solution to have very high *z*-axis accuracy to stay within the probes compliance range.

Additionally, with increasing multi-site counts, access of the probes to the dies on the wafer dictates feasible probe patterns. It is optimal to arrange the probes such that dies are accessed along a diagonal pattern (see Fig. 1). While this maximizes the probe connection access, it spreads the test sites over a distance that is increased by the √2 or 40% than if the sites were arranged in a direct row. However, a direct row arrangement severely limits probe access to the die. The z-axis planarity between the wafer (probe chuck) and the probe card must minimize angular z-errors to accommodate the z-axis compliance of the probes themselves. The probe card alignment system must provide accurate, repeatable alignment as probe cards are routinely swapped out. The alignment system must assure rapid, consistent changeover in the production environment.

It is also essential for the probe card and supporting mechanical structure to absorb the forces introduced by the increasing probe count.

If it is insufficient, deflection will occur when probes are compressed when making contact with the wafer. It is important that the support structure is both rigid and accurate so that proper contact force is made between the probes and the wafer. This force needs to be great enough to obtain the proper scrubbing action to break through oxides on the contact surface. It is also important that excess contact force is not required to overcome planarity errors as the excess force may damage structures on the die beneath the pads or can excessively deform solder balls.

By minimizing the tolerance loop from tester to wafer, *z*-errors can be maintained to 0.029 degrees, which is a factor of 2 better than what is required by multisite membrane probe solutions spanning up to 8 die of 8 × 8 mm, and even better for pogo based solutions.

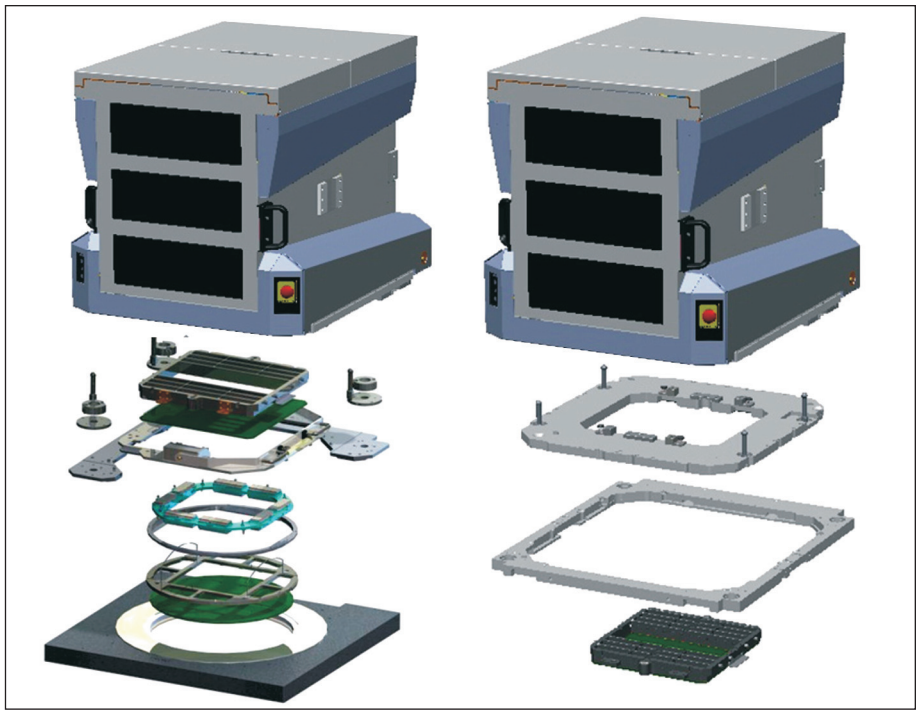

Figure 7 · Diagram comparing the old and new probe systems.

Rapid Changeover

In routine production, downtime is expensive, and unpredictable downtime is disruptive. Routine changeover of probe cards for a different device or for maintenance or repair must be quick to minimize downtime. Thus, minimizing the tolerance loop from probe tips to accuracy alignment features is essential to provide repeatable changeovers.

To address this, the process of changing the probe card should allow the test system interface to remain connected and aligned to the prober. A bottom-loading scheme is used to manipulate the probe card into place and align using unique alignment features in the design.

A modified bottom load probe card changer can achieve this. The production floor operator can remove and replace probe cards in the changer's loading tray. From there the loading operation is completely automated. The time required to place the probe card in the loader and have it planarized and locked in place is less than 5 minutes.

Summary

In summary, the cost and performance requirements of semiconductor devices used in consumer mobile electronics and other applications demand greater functional density and lower cost devices. These requirements are addressed with wafer level chip scale packaging. This in turn drives the need for full functional test at probe since traditional package and final test is eliminated from the manufacturing process. The physical constraints introduced by multi-site wafer level chip scale testing has presented challenges to traditional techniques used for interfacing the test system to the wafer prober. Innovative solutions that focus on reducing error sources and simplify tolerance loops can reliably and economically meet today's challenges at the performance levels required to test today's and tomorrow's complex semiconductor devices.

Author Information

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