Circuit Envelope Simulation: A Powerful Resource for 4G Power Amplifier Design

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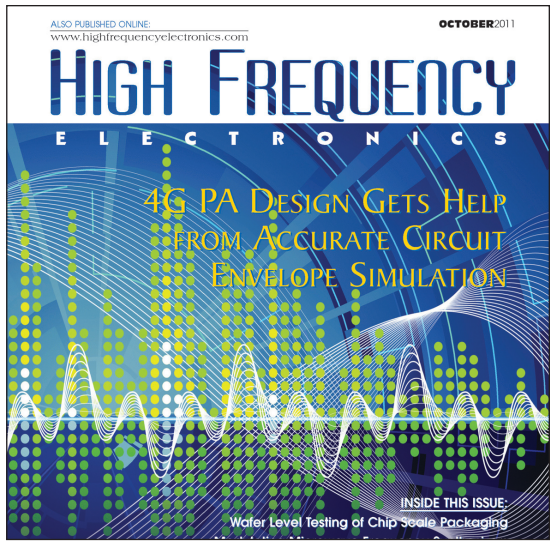
This issue's cover features AWR's circuit envelope simulation, which allows desginers to analyze how circuit design choices affect performance with modulated signals

Designers of RF power amplifiers for 3G and 4G wireless systems face conflicting challenges unlike those they have encountered before. For example, while today's higher-order modulation schemes require exceptional linearity throughout both transmit and receive signal paths, wireless carriers require the highest possible efficiency at the system level. Optimizing a circuit for one parameter invariably requires sacrificing performance of the other. Combine this and other unavoidable design conflicts with demands for greater instantaneous bandwidth and designers indeed have a conundrum. Achieving acceptable solutions requires not just standard time-domain and frequency-domain simulators but the unique contributions of circuit envelope simulation as well. This tool is seamlessly integrated within AWR 2011, and together with Microwave Office™ and Visual System Simulator™ (VSS) software, it can shave time from the design process while producing high-performance, manufacturable products.

The appeal of circuit envelope simulation results from its ability to more efficiently simulate complex digital waveforms than can time-domain and frequency-domain simulators such as harmonic balance (HB) and SPICE. The technique does not disregard the inherent advantages of these venerable simulators but rather builds on their unique characteristics by combining modulation data in the time domain and carrier signals in the frequency domain. It delivers a spectrum that



gives designers access to the modulation information (i.e. amplitude and phase) of every harmonic of the signal as they evolve over time. The result is the ability to analyze complex digitally-modulated waveforms fast and with greater accuracy than with the aforementioned simulators alone.

The further advantages provided by AWR's circuit envelope simulation result from its synergy with the other tools within the AWR 2011 Design Suite. That is, Microwave Office high-frequency design software incorporates thermal device effects and captures distributed design elements in a complete linear and steady-state nonlinear design suite. Its circuit representation flows seamlessly into the system-level environment of VSS, where circuit envelope simulation is then employed to monitor voltage and current waveforms in seconds rather than the minutes or hours required by transient solvers. With access to DC dissipated power as an output and any number of DC

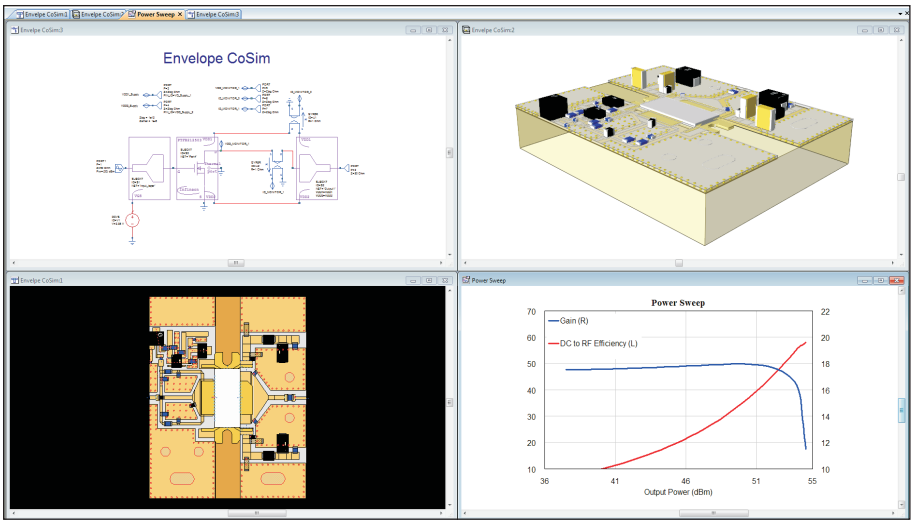


Figure 1 · Infineon power amplifier viewed within AWR 2011 (circuit envelope schematic, layout, 3D view and simulation results).

input pins to an underlying Microwave Office power amplifier circuit, VSS and circuit envelope simulation can enable complex active feedback, dynamic biasing, or MAC/PHY layer simulation scenarios.

Beyond Harmonic Balance

Harmonic balance is the basic nonlinear simulation engine for RF and microwave design, solving for nonlinear, steady-state voltages and currents in the frequency domain. As long as the signals of interest are periodic, HB engines are computationally efficient, very fast, and produce excellent results when provided with good models.

Harmonic balance, however assumes that the data stream is periodic. So, when simulating a complex modulated signal (common to modern digital communication systems) with an arbitrary bit stream, the period of the input signal must be at least as long as the stream of input data. When sampled appropriately, this leads to a huge number of spectral frequencies that must all be solved for simultaneously via HB techniques. Likewise, when simulating memory effects using HB simulation techniques for example, their aperiodicity must first be reformulated as a predictable signal. Corre-lation effects, not part of the actual physical phenomena, can then creep into the results and cause inaccuracies.

Another limitation of HB pertains to circuit/system-level co-simulation. When it is advantageous to include feedback within the system simulation—where the circuit simulation is controlled by the system simulation using previous circuit simulation time samples—this type of co-simulation simply cannot be performed with a steady state HB circuit simulator.

Enter Circuit Envelope Simulation

To capture dynamic operating phenomena such as memory effects, time-domain simulation is required, usually in the form of a transient, SPICE-type solver which, unlike HB, requires the entire waveform to be sampled. A 5 MHz-wide modulated signal on a 2 GHz carrier, for example, would require an integer multiple (N) of 2 GHz as a sampling frequency. If the simulated signal frame is 10 ms long, the simulation engine must simulate $N \times 2$ GHz $\times$ 10 ms = $N \times$ 2e7 samples to achieve results. While this will produce a solution, so many time steps are required that simulation speed slows to a crawl.

Circuit envelope simulation assumes that the input waveform has somewhat different characteristics. Unlike HB, time-domain techniques such as SPICE and circuit envelope can capture non-periodic dynamic operating-point information required for simulating memory effects. Rather than sampling the RF carrier, circuit envelope simulation samples only the modulation envelope. In the example above, this translates into $N \times 5$ MHz $\times$ 10 ms samples which is a 400x reduction in the number of time steps. Each time sample in a circuit envelope simulation is effectively solving the harmonic balance equations at the modulation carrier and related harmonic frequencies, so a single time sample in envelope is more expensive than a single SPICE transient time point (typically 10 to 100x slower) and thus a 400x reduction in time samples would result in a 4 to 40x improvement in circuit envelope simulation time versus that of SPICE. As the modulation bandwidth increases, the benefits of circuit envelope simulation will decrease, and for very wide band modulation, a SPICE type simulation will more than likely be faster.

Circuit envelope simulation is a perfect co-simulation match for VSS, which also samples the modulation envelope while creating, demodulating, and analyzing modulated waveforms such as GSM, EDGE, WCDMA, and LTE. Circuit envelope simulation lets designers place N-port Microwave Office circuit schematics directly into VSS system diagrams and simulate them to see how they behave in the presence of modulated waveforms. Dynamic voltages and currents and thus power-added efficiency can be of value weighted as well. The AWR software environment makes it possible to easily move between simulators and analysis techniques. Schematic elements corresponding to analyses and measurements can have multiple roles allowing linear, HB, transient, and circuit

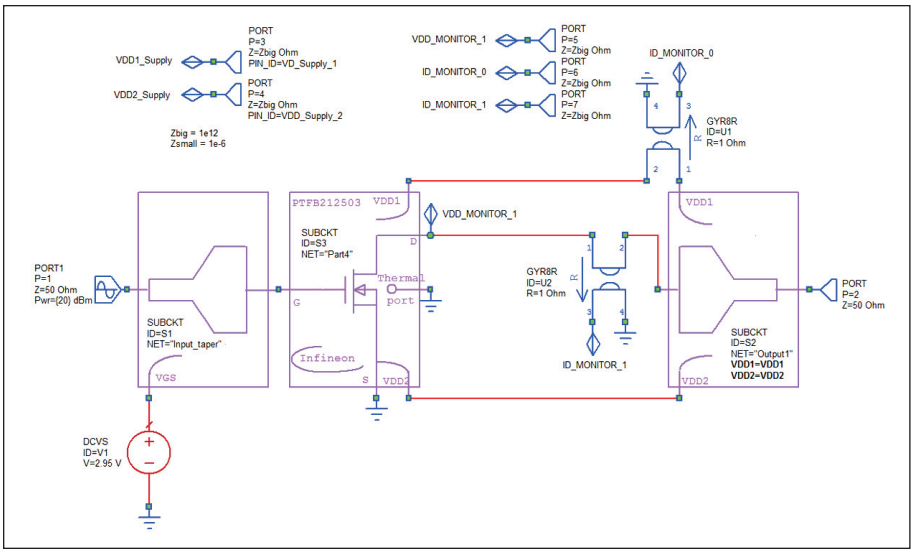


Figure 2 · Circuit envelope nonlinear simulation-based instance of Infineon power amplifier

envelope simulation to coexist in the same schematic.

As circuit envelope (Figure 1) is a time-domain technique, it is necessary to specify voltage and current probe-points on the schematic. Traditional input/output ports for the design are handled by PORT elements. Additional probes are also placed at the drain and in the DC bias path to supply DC voltage and monitor RF and DC voltage and current. Furthermore, since circuit envelope simulation is not restricted to the DC, fundamental, and harmonic elements of an HB analysis, the decision about where to place probes can be made based on much broader set of design criteria than signal sources and paths. The time-domain aspect of circuit envelope simulation allows design criteria like dynamic bias amplifiers, bias turn-down, or active equalization to be incorporated into the simulation as well.

Prior to incorporating the power amplifier in a circuit envelope test bench in VSS software, a hierarchical element must be created within Microwave Office. The "subckt" element representing the power amplifier design (Figure 2) has a typical PORT input driven by a source and a corresponding PORT output, but the element is augmented by five additional pins defined by the (NCONN)-named connectors: two voltage supply lines, one RF voltage monitor, one RF current monitor, and one DC current monitor.

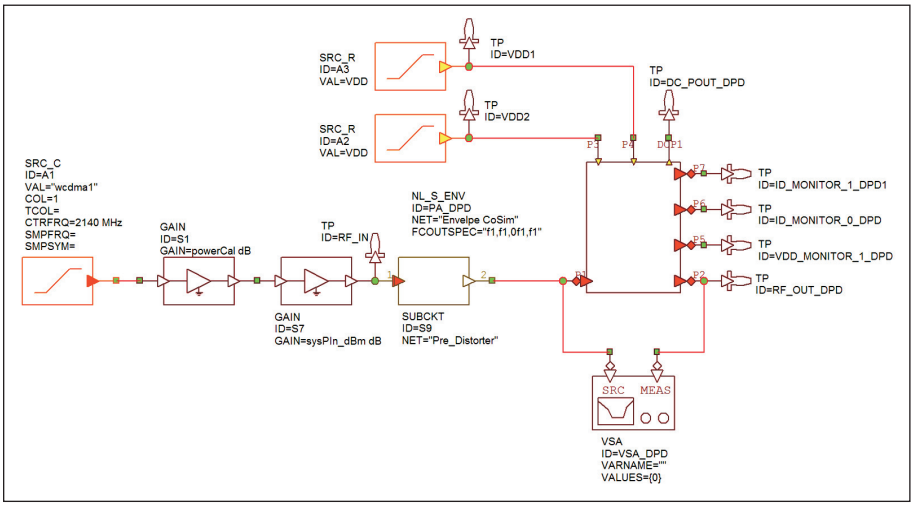


Figure 3 · Complete VSS diagram with circuit envelope co-simulation and predistortion.

Moving on to the envelope schematic, the complete power amplifier can be assembled from its constituent parts. The device within Microwave Office software can be combined with other elements such as digital pre-distortion, filtering, and antenna and channel models. Port definitions are added to the element to describe port functionality relative to the circuit simulation so the input port or ports, output ports, and DC or bias input lines can be controlled and monitored. Total DC power dissipation can be monitored as a separate port, calculated within the Microwave Office simulation, and then ported to VSS and circuit envelope for analyses of power-added efficiency and other DC-related parameters. The FCOUTSPEC parameter specifies the harmonic around which the envelope is to be simulated. Both RF and DC can be indicated for each of the output ports.

RF source and signal blocks combined with a Vector Signal Analyzer (VSA) block determine the simulation criteria. A voltage source is added to control the DC bias into the power amplifier, which in a more advanced design could be dynamic biasing, active time-domain circuitry, or MAC or PHY layer control, and even including feedback, because the voltage pin is within the VSS/circuit envelope time-domain environment. This is not available in linear or HB analyses alone. In Figure 3, a digital predistortion circuit precedes the power amplifier in the signal path to create a more efficient, highly-linear design solution that could not be designed with only a time-domain or

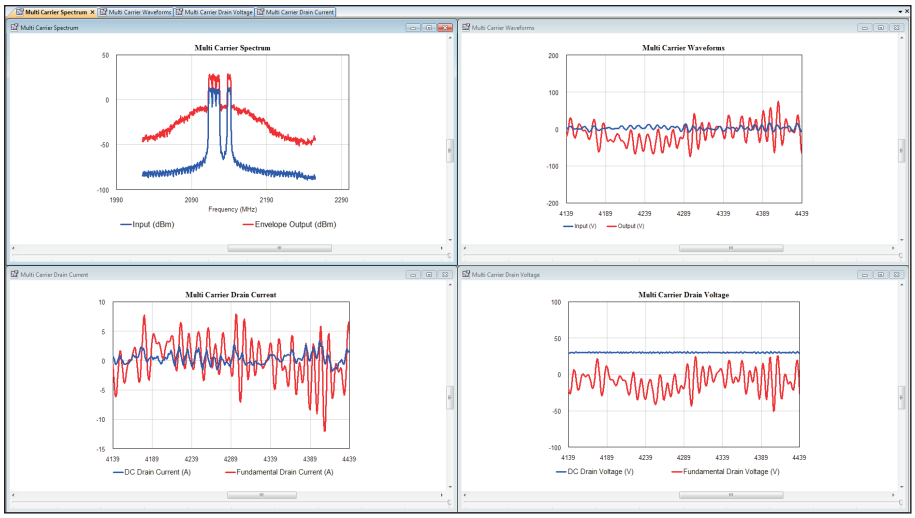


Figure 4 · Multi-carrier spectrum, time domain waveforms, as well as drain current and voltage for Infineon PA as simulated by AWR 2011 software featuring circuit envelope technology.

HB simulator.

The analysis results provide all the information required for system and circuit co-design without constraints on the simulation techniques used (Figure 4). Harmonic content, spectral masks, P_{in}-versus-P_{out} curves, and gain all can be analyzed with AWR's new circuit envelope technology. Additionally, these results can now be combined with time-domain analyses, such as collector current and voltage waveforms and RF perturbations of DC bias lines. Active turn-down through simulated control of DC pins can also be explored and analyzed. Waveforms and outputs are continually updated based on user-specified sampling and averaging criteria and can run real-time, which allows tuning and optimization within both Microwave Office and VSS software.

Summary

The stringent demands of the higher-order modulation schemes employed in today's leading-edge wireless systems make it essential that all ASP banks of RF power amplifier performance be taken into consideration. The integration of circuit envelope simulation within the AWR 2011 design suite and its seamless interaction with VSS allow designers to create amplifiers that deliver both high linearity and efficiency are of broad bandwidths that could not otherwise be achieved.

Acknowledgements

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Author Information

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