# A High Dynamic Range Receiver for the Radar Open System Architecture

By Frank Cannata MITEQ Inc.

This month's cover features an X-Band radar receiver for VMEbus applications, with high dynamic range and an adaptable design for use on other bands ME-based systems have been used for over 28 years as an open system architecture for processor and IO devices. Similar to the ubiquitous PC, The VERSAmodule Eurocard

bus (VMEbus) computer architecture was developed in 1980 to provide an open platform for any manufacturer to provide hardware that would conform to both the electrical specifications and mechanical form factor. The most recent version of the VME standard is VME64, offering improvements in bandwidth among other things.

While the availability of processor and I/O modules for VME have steadily increased over the years, high performance, digitally-controlled, microwave receivers remain highly customized for the specific application. For radar applications, high spurious-free dynamic range and pulse processing capabilities are important features of a microwave receiver.

A modular receiver chain has been designed at MITEQ compatible with the Radar Open Systems Architecture (ROSA) previously developed by MIT Lincoln Laboratory. The system employs VME based components to form and control the major functions of the radar. The receiver functionality conforms to the ROSA standard and can be used as an upgrade in a number of previously deployed radar systems.

In a typical radar system, multiple 3-slot wide VME-receiver modules are utilized in a single VME sub-rack to perform the function of a complete multi-channel receiver sub-system. Details of an X-Band receiver, one of the



Figure 1 · The MITEQ radar receiver was developed for VMEbus applications.

more common radar bands, are presented in this article as an example. Other bands—S, C, Ku, etc.—can be configured with the same receiver architecture. A block diagram of the receiver is presented in Figure 2.

### **X-Band Receiver**

The MITEQ X-Band receiver is of a dual conversion superheterodyne architecture that translates a 10 GHz signal with a bandwidth of 1 GHz to an IF center frequency of 70 MHz and a bandwidth of 20 MHz for stretch processing of radar returns. The receiver also includes a wideband IF output at 1 GHz for use with advanced high speed ADC (analog to digital converter) processing techniques such as optical processing, time sequenced ADC arrays, or time stretched ADC arrays.

The receiver employs a VMEbus digital interface that facilitates control and monitoring on a pulse-by-pulse basis, as well as channel gain and phase adjustment for system calibration purposes. A block diagram of the receiver's digital control sub-system is shown in Figure 3. A Xilinx CPLD (complex pro**High Frequency Products** 

# VME RADAR RECEIVER



Figure 2 · X-Band radar receiver block diagram.



Figure 3 · The radar receiver's digital subsystem.

grammable logic device) is used for interface and control logic for the receiver's monitoring and control functions. This architecture provides a growth path for the receiver to be reconfigured without hardware changes.

# Peak Pulse Detection and Delayed AGC

A built-in SDLVA (successive detection log video amplifier) provides detection of the filtered IF output signal over an 80 dB dynamic range, and an on-board ADC digitizes the video signal and performs peak detection within a gate (or windowing) pulse signal provided by the radar platform. The resulting peak is read by the system between pulses, which subsequently commands the on-board gain control over the VMEbus to set the receiver's sensitivity for the next pulse, a process commonly referred to as delayed AGC.

The receiver has a second onboard ADC that digitizes four built-in test monitoring signals; RF, IF, LO1 and LO2 signal detectors. Values for these four signals are read by the system over the VMEbus for diagnostic purposes.

#### **Digitally Calibrated Attenuator**

Gain control for the receiver is provided by a voltage-controlled microwave attenuator. The attenuator is driven by an on-board DAC (digital to analog converter). The attenuator provides 40 dB of additional dynamic range for the receiver, and is capable of being set prior to reception of each radar pulse to optimize the dynamic range of the system. As the target approaches, the system will sense higher peak signal strength, and then reduce the receiver's gain.

Accurate calibration for the gain control attenuator is very important for system accuracy and stability. Since most analog-based microwave control components have inherent nonlinearities, they must be linearized with either analog and/or digital circuits. In this receiver, digital calibration was used to achieve accurate linear operation of the gain control attenuator. An EEPROM (electrically erasable, programmable readonly memory) was used to store calibration data. The EEPROM is programmed "in-circuit" at the factory when the receiver is under test. Calibration software is used to control an external network analyzer to characterize, program and verify the RF performance of the gain control attenuator through the PROM-DAC pair. A typical plot of attenuation accuracy before and after calibration is shown in Figure 4.

Two additional PROM-DAC pairs are provided in the receiver for calibration of phase and amplitude at the system level. An analog phase shifter with 360 degree range, and a second attenuator with 15 dB of range provides fine tuning capability for the radar system's channel-to-channel phase and gain offset.

#### High Dynamic Range Front-End

The X-Band receiver employs the use of an hermetically sealed multichip module LNA (low noise amplifier) that integrates MMIC and discrete components selected for an optimal selection of Gain, Noise Figure, and Compression Point. A dual MMIC device LNA was used where a **High Frequency Products** 

VME RADAR RECEIVER



Figure 4a · Uncorrected gain control attenuation vs. DAC input word.



Figure 5 · Phase variation vs. attenuation performance of the phase invariant gain adjust attenuator.

low noise stage is cascaded with a medium power stage to meet the system dynamic range requirements.

#### **Termination Insensitive FET Mixer**

The receiver also employs a MITEQ high IP3 termination insensitive mixer (TIM). The high intercept point is provided by a dual FET architecture that is surrounded by 90 degree hybrid couplers. The coupler terminations help reduce the sensitivity of the mixer response to external termination impedances, improve input compression of the mixer, and provide cancellation of the even-order intermodulation products. The mixer has an input third order intercept performance of +33 dBm and a conversion loss of 9 dB.

# Phase Invariant Gain Adjust Attenuator

The receiver's gain adjustment attenuator, used for system gain trimming, is designed to maintain constant phase versus a 15 dB attenuation range. Phase change is under 2 degrees as shown in Figure 5. The attenuator utilizes PIN diodes selected to offer high intercept point to



Figure 4b · Attenuation error vs. attenuation for the digitally corrected gain control.

prevent the generation of third order spurious products. The attenuator architecture further minimizes the nonlinear control voltage vs. attenuation transfer function. This eliminates the need for analog linearizers, while still maintaining very good accuracy using the PROM-DAC calibration scheme.

#### IF Conversion/Log Video Module

An integrated IF conversion and Log Video module was designed for this receiver to provide all functions from the second IF conversion through to the final IF output and log video outputs. The module incorporates a phase shifter on the LO2 signal for system phase adjust, LO2 and IF output signal monitors, 80 dB range Log Video detector, and final analog filtering at a 20 MHz bandwidth provided by a SAW filter.

#### In Conclusion

A high performance radar receiver has been developed for use in a flexible radar open architecture VME system. The receiver provides high dynamic range and pulse processing capabilities demanded by modern radar systems, with a true VMEbus interface that allows the device to be easily integrated into existing and future radar systems.

#### Author Information

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