

# Design Suite Provides Advanced Technology for Analog and RFIC Design

By Tom Quan  
Applied Wave Research, Inc.

This new EDA design system allows an IC designer to develop new products more quickly, and with improved first-time success, by integrating circuit level and physical level simulation and analysis

Over the past 20 years, EDA tools have evolved primarily as isolated activities for each phase of a design. Legacy systems separated the electrical design and analysis from the physical implementation at the IC, package,

module and printed circuit board (PCB) levels. EDA vendors have developed closed methodologies and tool sets for different portions of the design process, requiring manual hand-offs and multiple iteration loops that result in costly errors and delays. The complexity of today's new semiconductor process technologies, as well as module implementation technologies, however, renders these traditional design methods inadequate in terms of accuracy, efficiency and cost.

The high-frequency circuit impairments in today's complex analog and RF ICs, such as compression, noise, distortion and phase noise, as well as the physical parasitics like interconnect impedance and coupling, are forcing the need to obtain complete "RF closure" between the RFIC's system and circuit, electrical and physical, and design and test activities before commitment to costly IC implementation.

Applied Wave Research, Inc. has focused its research and development effort on an advanced software architecture with a unique core technology—a modern object-oriented data model that is inherently open and flexible. AWR's Analog Office 2004 design suite provides an entirely new approach that achieves optimum RF closure through a uni-

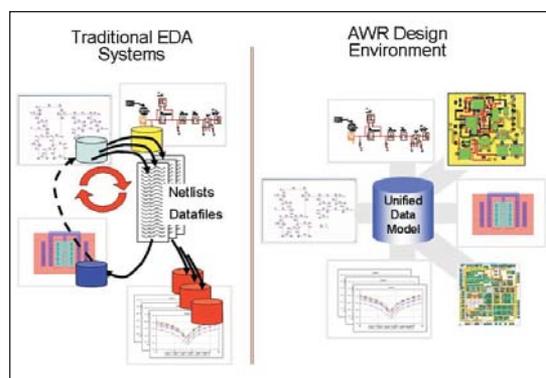
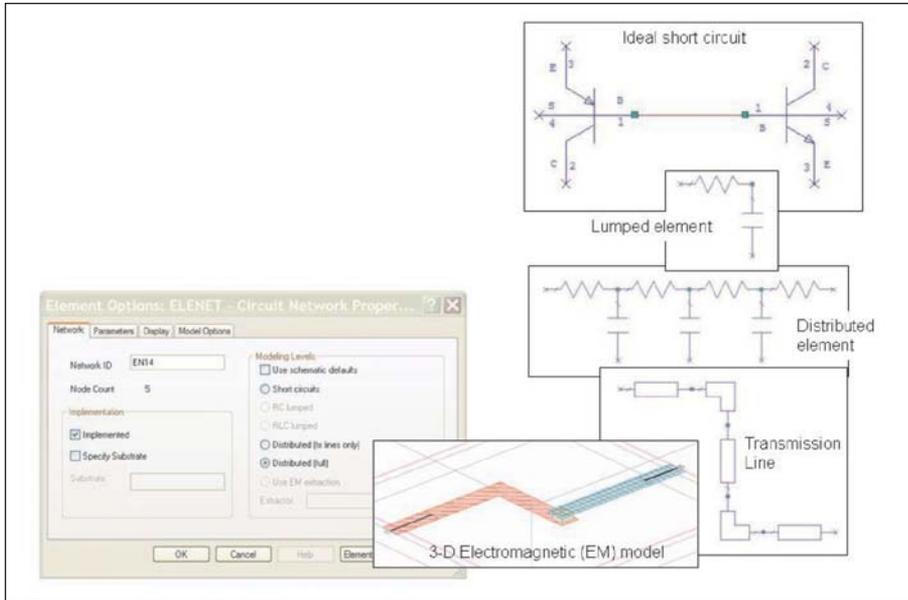


Figure 1 · AWR's Analog Office 2004 design system provides a new approach that achieves optimum RF closure through a unified data model and design environment encompassing all of the design domains.

fied data model and design environment encompassing all of the design domains. The data model is high-frequency aware, permitting accurate extraction and modeling of all design elements, including active and passive devices as well as interconnects, at high frequency. The new solution is built on an open, standard-based software platform, enabling easy integration of the most capable, best-in-class tools to capture, synthesize, simulate, optimize, layout, extract, and verify designs in all domains. The Analog Office design suite is fully integrated into existing digital and mixed signal IC design flows and enables analog and RFIC design engineers to significantly shorten their development cycles and speed wireless products to market.

AWR's open software architecture and industry-standard application programming interface give customers easy access into the



**Figure 2** · Analog Office 2004 software offers an interconnect-driven/RF-aware methodology that focuses on accurate RF interconnect modeling and analysis throughout the entire RFIC design.

underlying data structures, allowing seamless integration with other best-in-class tools and design environments. This protects customers' investment in models and simulators, lowers their cost of support, and enables easy customization of specific flow requirements (see Figure 2).

### Concurrent Interconnect-Driven/RF-Aware Design Methodology

Analog Office 2004 software offers an interconnect-driven/RF-aware design methodology built around AWR's Intelligent Net™ (iNet) technology. Similar to timing-driven or wire-driven digital design methodology, the interconnect-driven/RF-aware methodology focuses on accurate RF interconnect modeling and analysis throughout the entire RFIC design process to reduce or eliminate design iterations, shorten the design cycle, and ensure first-time design success. Unlike existing net constructs built on a "digital-centric" data model, the Analog Office 2004 iNet technology is based on an RF-accurate net model with multiple levels of abstraction—"short-circuit," lumped RLC, dis-

tributed and coupling resistors, inductance, RLCK, fully distributed transmission line, or full 3-D EM models—using a single environment and data model. iNet technology provides concurrent and real-time physical modeling of RF interconnects while the layout is in progress, eliminating the need for a serial post-layout connectivity extraction step. Simulation and analysis can be invoked immediately to verify the performance of the design as soon as the critical nets are laid out, without waiting for the rest of the circuit to be completed, ensuring early and complete RF design closure.

### Complete Front-to-Back Analog and RFIC Design System

The Analog Office 2004 unified design environment fully interacts with a comprehensive and powerful set of integrated tools for top-down and front-to-back analog and RFIC design. The toolset spans the entire IC design flow, from system-level to circuit-level design and verification. An easy-to-use graphical user interface supports system- and circuit-

level design methodologies, electrical and physical design, schematic capture, simulation/analysis, layout and verification, frequency- and time-domain simulation and analysis, and links from design to test. The integrated waveform display and analysis capabilities support complex RF measurements, including hundreds of pre-built measurements, parametric tuning, noise analysis, sweep parameter analysis, multiple test benches with multiple simulators, statistical analysis, and optimization.

A variety of simulation types are offered, including system simulation with AWR's Visual System Simulator™ (VSS™), time-domain simulation with Synopsys' HSPICE®, frequency-domain simulation with AWR's harmonic balance simulator, and electromagnetic simulation with AWR's EMSight™. The open platform provides third party tool integration through a SPICE socket for third party SPICE-based circuit simulators and AWR's EM socket™ for third party EM simulators.

The software also offers a powerful and easy-to-use physical design suite with a fully interactive layout editor supporting polygon editing and parameterized layout cells, automated device-level placement and interconnect routing, an integrated and interactive design rule checker (DRC), and 3-D full field solver-based extraction with industry gold standard, high speed extraction technology from OEA International.

### Measurement-Driven Paradigm

Analog Office 2004 design suite has pioneered a new, yet more natural, paradigm for high-frequency design. In traditional EDA systems, users must undergo multiple design setup steps to obtain a particular analysis result from a selected simulator, resulting in the generation of many data files. In Analog Office 2004, however, users simply set up multiple test benches and analysis measurements ahead of time (similar

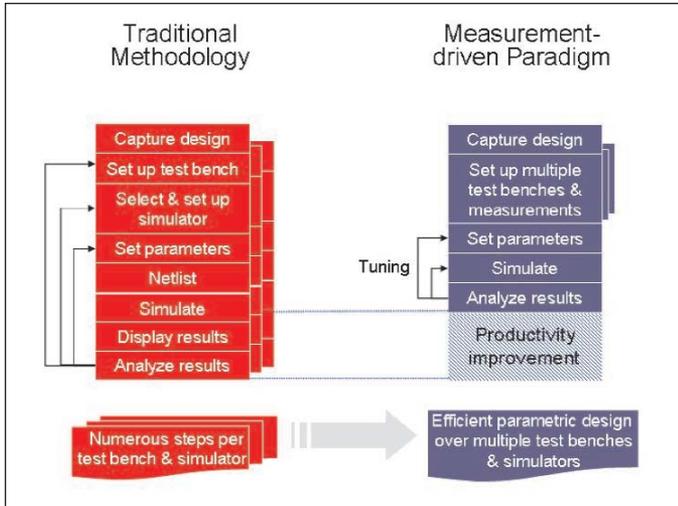


Figure 3 · A new measurement-driven paradigm provides efficient parametric design over multiple test benches and simulators, shortening design time.

to a specification sheet) and then set up the parameters for the designs. As soon as the simulation is started, the system automatically selects the “right” simulator for the particular analysis, extracts the “right” models for the design elements, runs the simulation(s), obtains the results and processes them into requested measurements, and presents the results in multiple graphs and tables. In the same environment, users can dynamically “tune” the design across a set of parameters, test benches, and simulators quickly and efficiently. Figure 4 shows the plots representing the design results for a power amplifier.

**Powerful Analog and RF Simulation Technologies**

AWR provides one of the industry’s fastest harmonic balance simulators, which performs 10 to 1000 times faster than similar products for most problems. This improved simulation performance is coupled with proprietary convergence algorithms that extend the capacity of the simulator to handle large and highly nonlinear circuits. The superior speed and capacity of the simulator allows designs to be subjected to more rigorous statistical modeling and yield analysis, making these valuable processes practical for circuits that may have consumed too much simulation time in the past.

The Analog Office 2004 time-domain simulator is able to solve unique problems such as those found in phase-locked loops or oscillators during start-up conditions. An optional time-domain engine, which augments the harmonic balance, Volterra and EM simulators, is integrated with Synopsys’ golden standard HSPICE, which provides fast, accurate, high capacity simulations, aided by hundreds of foundry-proven built-in device models for most commercial integrated circuit (IC) foundries.

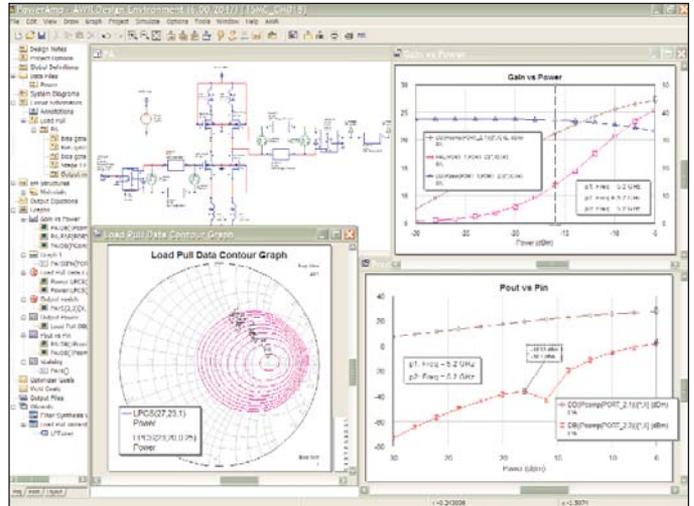


Figure 4 · Detailed design and analysis results are shown for a power amplifier, including gain vs. power, pout vs. pin, and load pull data contour.

**Design Kits Support Popular Silicon Foundries**

The integrity of the electrical and physical model data is often a contentious issue between foundry customers, foundries, and EDA vendors. Neither an EDA company nor a foundry can deliver an optimal PDK in isolation.

Initially driven by mutual customers, AWR has established close partnerships with leading RFIC foundries to develop and deliver validated process design kits (PDKs) for SiGe, BiCMOS, and RF CMOS processes that include integrated electrical models, including schematic symbols and simulation models, parameterized layout cells, and design rule check (DRC) files, enabling an efficient and error-free RFIC design flow. End users, commercial foundries, and EDA ven-

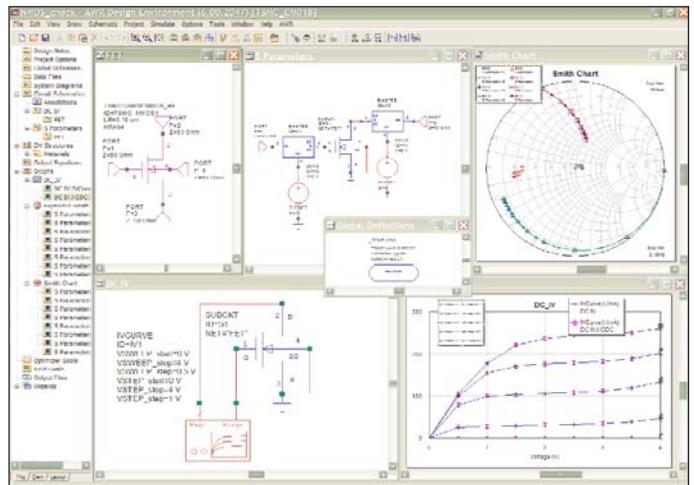


Figure 5 · Open, standard-based process design kits support popular silicon foundries for an efficient and error-free RFIC design flow.

dors can all benefit from the reduced support effort, higher customer satisfaction, and shorter design cycles that result from integrated foundry libraries.

### **A Full Set of Physical Layout Tools**

Analog Office 2004 design suite provides IC designers with a complete physical design system to fully implement their analog and RFIC designs within a single environment, eliminating the need for switching between multiple environments and databases.

A fully interactive custom layout tool with integrated device-level, auto-placement and auto-routing features speeds up the creation of analog and RF circuit blocks and chips. A fully integrated DRC ensures the physical layout being created always meets the process design rules, resulting in a correct-by-design, error-free layout. The layout editor is directly connected to the EM socket, providing "on-the-fly" EM extraction and modeling of arbitrary layout structures and complex spiral inductors. At every step during the physical design process, the iNet technology continuously updates the underlying interconnect data model in real time, and as soon as each interconnect is "implemented" or laid out, concurrent simulation and analysis can be immediately invoked on schematic or layout to verify the performance of the overall design without waiting for the final layout of the whole design to be completed.

To ensure proper modeling of inductive coupling between nets in GHz physical layout, the software also provides the Cheetah 3-D field solver, the core interconnect extraction technology from OEA International's NET-AN™ 3D critical multi-net field simulator. The selected net or nets are automatically extracted and modeled as distributed RLCK for fast and accurate simulation. This level of interconnect modeling compliments other modeling levels that are managed by iNet technology, such as lumped RLCs, and fully distributed transmission lines, thus extending the designer's range of design trade-off flexibility between simulation run-time performance and modeling accuracy.

### **Seamless Integration with Cadence's Mixed-Signal IC Design Flow**

Analog Office 2004 design suite can be used to design the entire chip from system-level modeling and simulation through to final layout and tape-out. The software will generate the necessary industry-standard files, such as layout vs. schematic (LVS) netlist and GDSII, to interface to a final verification flow based on industry-popular IC physical verification tools from Mentor Graphics, Synopsys and Cadence.

Complete RF blocks can also be designed as part of a large mixed-signal system-on-chip (SoC). In this flow, the software provides complete, bidirectional data transport capabilities to and from standard industry mixed-signal IC design flows, including Cadence's Design Framework II-based analog/mixed-signal flow, for full chip assembly, physical verification, and tape-out. The data transport solution currently supports Cadence Virtuoso® custom design platform, including Composer schematic editor, Analog Design Environment or ADE (formerly Analog Artist), and Virtuoso layout editor. The solution transfers full Composer schematic data, such as schematic symbol graphics, interconnect wires, connectivity information, component properties, schematic and global equations, and a host of other specific ADE data. The data transport solution can also transfer layout data between Analog Office 2004 and Virtuoso layout environment while maintaining parameterized cell (Pcell) information and mapping. An LVS netlist can be generated from Analog Office 2004 for final verification in the Cadence design environment.

AWR is actively working with OpenAccess to ensure a smooth path between Analog Office 2004 design system and an OpenAccess-based Cadence design flow. The resulting integrated flow is similar to the current Analog Office and Cadence Design Framework II integrated flow, except that OpenAccess is now the common database.

### **Summary**

Performance issues in modern communications applications, such as the use of complex modulation schemes and the demand for high power efficiency, plus the constant demand for low cost, is driving a growing need to achieve complete RF closure in a design before commitment to costly implementation. Designers need to be able to examine a device's behavior in both the time- and frequency-domains in an efficient way. Analog Office design suite provides the unique ability to streamline the RFIC design process by combining within a unified, easy-to-use environment both system- and circuit-level design phases. This includes both time- and frequency-domain simulation capabilities, as well as models, libraries, and measurements that are completely compatible and seamless between those system and circuit design phases and the frequency- and time-domain engines. For more information on Analog Office 2004, contact:

**Applied Wave Research**  
**Tel: 310-726-3000**  
**[www.mwoffice.com](http://www.mwoffice.com)**  
***HFeLink 301***