Wireless Receiver Design Emphasizes Direct Conversion

From the earliest work on rectifiers to detect spark transmissions to advanced low-noise semiconductors for deep space research, receiver design and component innovations have enabled many advances in communications technology. With the vast majority of current wireless systems employing digital transmission, the simplicity and low implementation cost of direct conversion receivers has brought that technique to the forefront.

With digital signals, the shortest path from the analog RF input to a digital signal ready for processing is highly desirable. Direct conversion translates the radio frequency of a signal to an equivalent bandwidth centered on DC (or zero Hz). At this low frequency range, the most inexpensive digital IC technology can be used for processing. Since power consumption of digital devices increases with clock frequency, baseband processing requires the least power for its operation.

As is often the case, the advantages of any design approach may also present new design challenges. In a direct-conversion receiver, the advantage of eliminating IF stages means that the local oscillator is at the center frequency of operation. Exceptional balance and reverse isolation performance is required to avoid excessive radiation of the LO via the receiving antenna.

Conversion to a "DC" baseband can result in a significant DC component in the output to the analog-to-digital converters. Although some applications can accept a bandwidth that filters out this DC component, many do not, so it must be minimized.

These performance issues of direct-conversion receivers are reviewed in the article that follows this report, which extends the discussion to the specific effects of intermodulation distortion products.

	ADVANTAGES	DISADVANTAGES
Superhetrodyne:		
	High selectivity easily obtained	High performance IF filter(s)
	High dynamic range easily obtained	May have multiple LOs
	Can operate at any frequency	Most complex RF architecture
Direct-Conversion:		
	Single LO	Requires high performance front-end
	Simple architecture	Potential DC offset problems
	Wide frequency range	Potential for LO radiation
Direct-to-Digital:		
	Lowest RF component count	RF performance challenges
	Handles very wide bandwidth	Limited frequency range
	Flexible configurations	Needs low-jitter, high frequency clock

Some comparisons among current receiver methodologies.

Next Generation Direct-to-Digital Receivers

Although it is possible to connect an analog-to-digital converter (ADC) directly to an antenna, few applications currently use this technique. The performance demands for a true "antenna-to-ADC" receiver are sufficiently high that, at present, system performance is more easily achieved using direct-conversion to baseband.

However, it also seems correct to suggest that direct-to-ADC detection is actually the same function as the separate RF and digitizing circuits used in direct conversion. After all, the ADC has a high performance analog front end to condition the input signal, and the threshold detection circuits of the digitizer are more accurately characterized in the continuum of analog signals than the on-off states of digital signals. Thus, a direct-to-ADC receiver simply integrates an RF front end into a digital device with less interface circuitry between them.

In one respect, a step towards integrated RF/digital signal detection has already become commonplace. In present RF mixer/detector technology, the highest performance is obtained with switch-mode configurations that require both frequency domain and time domain analysis for their characterization.

Still, this new topology will present designers with additional challenges. The system clock will now perform the LO function and must have the kind of low phase noise (jitter in the time domain) performance of present RF circuits. Instead of baseband, the operating frequency will be presented to the ADC, which puts high frequency analog signals on-chip with high frequency clocked circuitry. These factors, along with other high frequency/high speed design issues, are the types of tasks being addressed for future receivers.

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