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Noise Reduction in Transistor Oscillators: Part 2—Low Frequency Loading and Filtering

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Part 2 of this three-part series presents several techniques for the reduction of noise by optimizing the design of the circuitry

Optimization of low frequency loading and feedback circuit can help minimize the 1/*f* noise in the transistor oscillators. In a first approximation, a gate voltage noise generator connected in series with a noise-free nonlinear two-port circuit can model the low frequency 1/*f* noise in FET devices. So, if the low-frequency voltages applied to gate-source and drain-source terminals are reduced, the resulting sideband components around the oscillation frequency due to nonlinear mixing of these voltages will be reduced as well. To realize such an approach, it is necessary to provide the short-circuiting of the drain port and open-circuiting of the gate port at low frequencies [11]. The phase noise improvement under these conditions was verified experimentally by connecting external variable resistances R_g and R_d to the gate and drain ports, as shown in Figure 13(a), where C_b are the blocking capacitances. The minimum phase noise conditions are realized for ideal case when $R_g = \infty$ and $R_d = 0$. This means that, in practice, a high value of external resistance R_g at low frequencies is needed when it is bypassed by the choke inductance L_{ch}, and no converted noise variations will be observed.

It was found that 1/*f* noise could be approximated by a quasi-stationary phenomenon having a quasi-constant autocorrelation function [12]. Consequently, it is possible to reduce phase noise by applying a feedback voltage in series with the 1/*f* noise generator using parallel resistor R_f shown in Figure 13(a). The higher voltage gain from input to output, the stronger feedback may be applied and the lower variations of the gate-source voltage can be observed. The low frequency feedback circuit is also capable of canceling thermal noise at low frequencies. The amount of cancellation is determined by the circuit delay and the frequency. Due to gate and drain loading, an 8 dB phase noise improvement can be obtained at 1 kHz offset from the carrier for 10 GHz microwave oscillator. Optimizing the values of the gate, drain and feedback resistances results in overall 11 dB phase noise improvement with optimum values of $R_f = 0$, $R_g > 100$ Ω and $R_d < 100$ Ω [11].

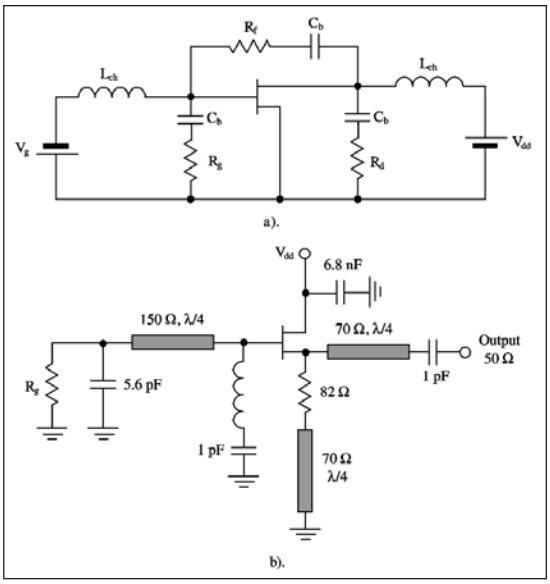

Figure 13 · Diagram of a low frequency circuit reducing phase noise.

Figure 13(b) shows the circuit schematic of a common drain microwave MESFET oscillator with a direct current resistor R_g between

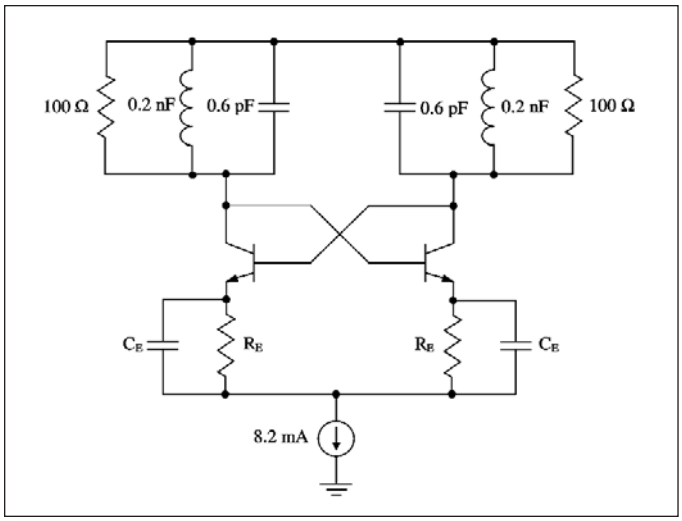

Figure 14 · VCO topology incorporating emitter degeneration.

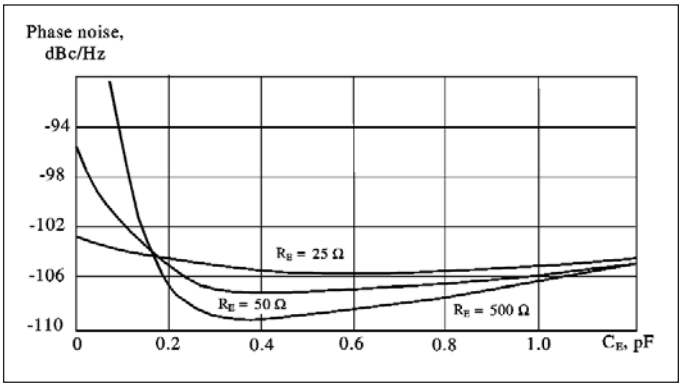

Figure 15 · Simulated phase noise of *LC* oscillator with emitter degeneration.

the gate and the ground [13]. This low-frequency resistor, bypassed at high frequencies, also affects the noise upconversion by allowing the gate rectification current to produce an optimum reverse bias on the gate. The lowest phase noise was obtained when a gate resistor R_g = 1 kΩ was used in the 5.6 GHz oscillator and a gate resistor R_g = 200 kΩ was used in the 7.4 GHz oscillator providing a 14 dB noise reduction. Thus, there is an optimum value of the bias voltage minimizing the oscillator phase noise. In order to obtain low phase noise at low offset frequencies with dominating 1/*f* noise, the bias point should be chosen to avoid the increasing output conductance at the transition between the active and saturation regions, as well as operation in the pinch-off region should be minimized corresponding to a Class AB mode with high quiescent current [14]. Within these limitations, it is necessary to maximize the oscillator output power. To keep the MESFET device operating in active region, the technique utilizing a pair of limiting diodes can be used [15]. Two limiting diodes are placed between the source of the MESFET device and resonator to clip the oscillation amplitude before driving the transistor into nonlinear operation. Although adding a pair of diodes introduces new nonlinearities in the circuit, overall 1/*f* noise will be reduced since the MESFET is operated in a linear active region and the diode nonlinearities are small compared with those of the MESFET device.

Figure 14 shows a typical LC oscillator circuit based on a cross-coupled transistor pair incorporating emitter degeneration [16]. The proper choice of the parameters of the oscillation circuit provides the tuning range from 12 to 15 GHz using bipolar devices with transition frequency f_T = 45 GHz from SiGe 6HP process. The oscillator phase noise at 2 MHz offset is illustrated in Figure 15. If degeneration capacitance C_E is too small, the noise generated by the feedback resistance R_E is not adequately filtered resulting in noise degradation. For a degenerated VCO with R_E = 300 Ω, varying capacitance C_E from 0.3 to 0.8 pF provides a tuning range of the oscillation frequency from 14.6 to 12.6 GHz. The optimum combination of the values of the degeneration resistance R_E and capacitance C_E improves the phase noise performance by approximately 7 dB compared with the non-degenerated design.

The experimental results show that, when using a negative feedback from unbypassed emitter resistance in a bipolar oscillator, effects of the flicker noise upconversion can be significantly reduced [17]. Theoretically, it can be explained by the linearization of the device transfer function when DC and fundamental components of the collector current become the linear functions of the base voltage beginning from their very small values. This leads to the significant reduction of the low frequency noise-to-carrier modulation or flicker noise upconversion. However, a high value of the unbypassed emitter resistor

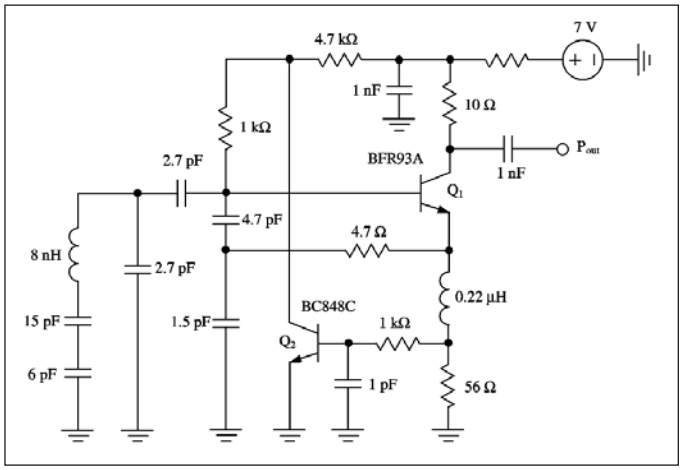

Figure 16 · Bipolar oscillator schematic with emitter noise feedback (18).

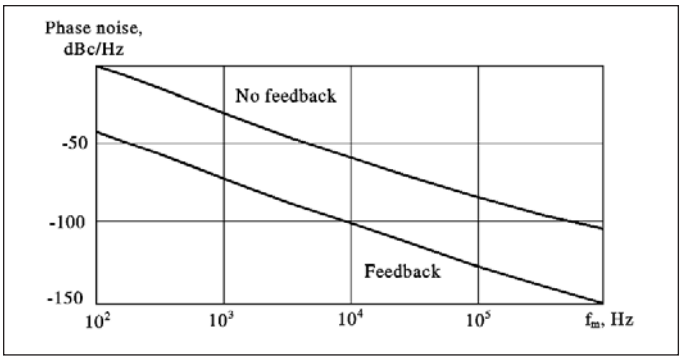

Figure 17 · Phase noise of bipolar oscillator with and without feedback.

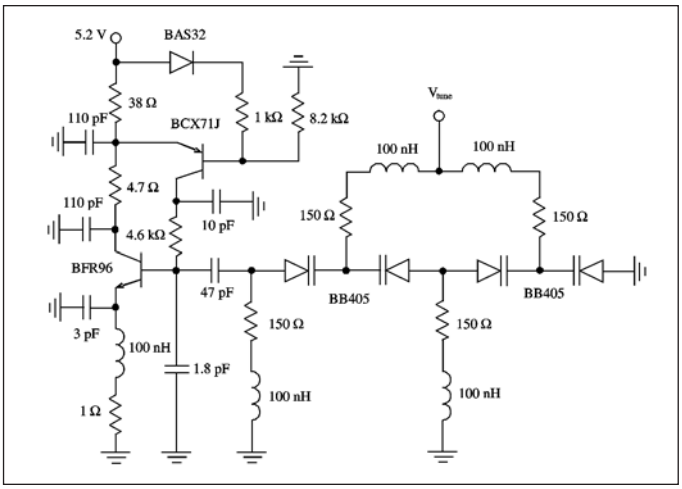

Figure 18 · Bipolar oscillator schematic with collector noise feedback (20).

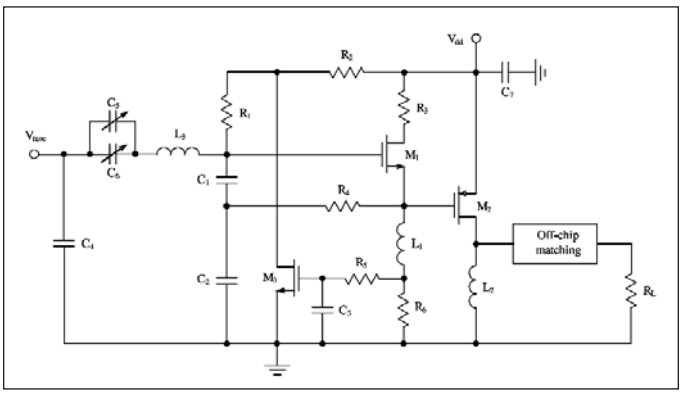

Figure 19 · CMOS VCO with low frequency feedback (21).

reduces also the active device transconductance resulting in lower output power and regeneration factor. Therefore, it is preferable to use the emitter resistance together with a noise feedback circuit. Figure 16 shows a bipolar oscillator schematic with emitter noise feedback [18-20]. Due to the feedback loop, the noise across the emitter resistor is sampled by a sampling transistor, inverted, amplified and fed back into the base of the RF transistor.

The simulation results shown in Figure 17 demonstrates about 40 dB phase noise improvement for a perfect phase shift of 180 degrees at the oscillation frequency of 1.2 GHz. The same result can be achieved using noise sampling from the collector resistance shown in Figure 18 [20]. This voltage-controlled oscillator provides a frequency tuning range from 612 to 1,124 MHz within the varactor bias voltage range from +1 to +22 V. Since the bandwidth for a single transistor can only be about 1 MHz with guaranteed phase shift close to 180 degrees, practical circuits can show a noise improvement between 15 and 20 dB.

A fully integrated RF CMOS VCO with on-chip low frequency feedback loop for flicker noise suppression is shown in Figure 19 [21]. Here, the emitter resistance R_6 first samples the low phase noise from DC current. Then, a low-pass filter represented by a resistor R_5 and a capacitor C_3 is used to suppress the high frequency components appeared across the emitter resistor R_6. The sampling nMOS transistor M_3 provides 180-degree inversion, amplification of the low phase noise signal and its final delivery to the gate of the nMOS transistor M_1 through the resistor R_1. The capacitances C_1 and C_2 form a positive feedback loop to provide the negative resistance resulting in the start-up and steady-state oscillation conditions. The LC tank consists of the inductor L_3 with a quality factor around 10 at 5 GHz and the varactors C_5 and C_6 with a tuning range from 0.65 to 1.4 pF within 2 V voltage range. The resistors R_1 and R_3 provide the biasing of the MOS transistors. The inductor L_1 serves as RF choke. The pMOS transistor M_2 and inductor L_2 are the components of the buffer amplifier. Being implemented in 0.18 μm CMOS technology, such a VCO with low noise feedback loop provides the output power of 15 mW at supply voltage of 1.8 V, the frequency tuning range of 6.1% around the center frequency of 5.74 GHz and the phase noise of –69 dBc/Hz at 10 kHz offset and –98 dBc/Hz at 100 kHz offset. The size of chip area is 1.6 × 1.5 mm^2. It should be noted that using such a low noise feedback loop enabled the phase noise reduction by 4–6 dB.

Filtering Technique

The current source in the differential LC oscillators is required to set the bias current and provides high impedance in series with the switching active devices of the differential pair. In a perfectly balanced circuit, odd harmonics circulate in a differential path with no current flowing through the current source (out-of-phase operation). At the same time, even harmonics flow in a common-mode path through the active devices, resonator cir-

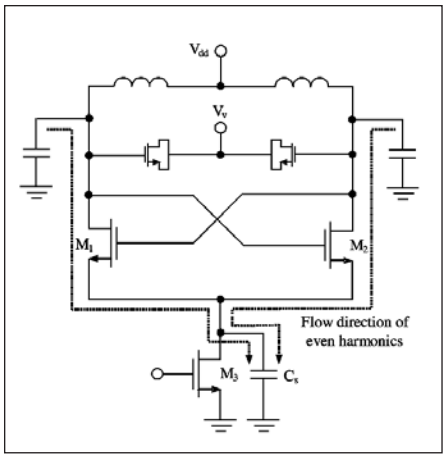

Figure 20 · Differential tail-biased VCO with capacitive noise filter.

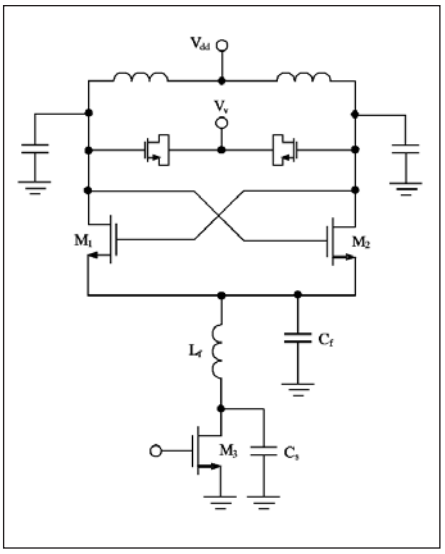

Figure 21 · Differential tail-biased VCO with complete noise filter.

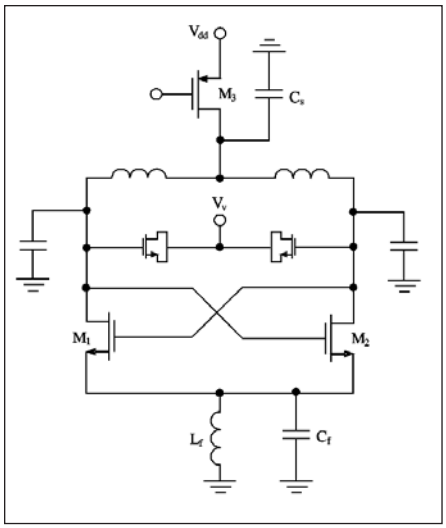

Figure 22 · Differential top-biased VCO with complete noise filter.

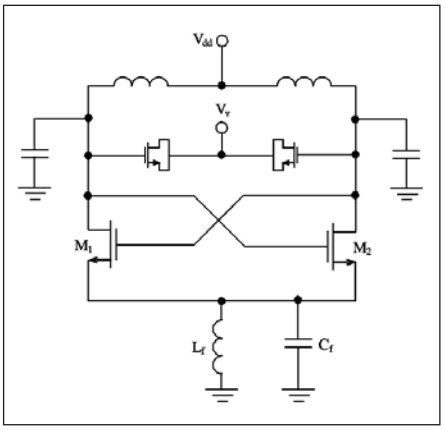

Figure 23 · Differential voltage-biased VCO with noise filter.

cuit and current source (in-phase operation). Because of the mixing effect provided by the nonlinearities (nonlinear transconductance and intrinsic capacitances) of the oscillator transistors, the low frequency noise of the current source is initially upconverted to high frequency noise around even harmonics and then downconverted to the phase noise around the fundamental. Since the level of the third- and higher-order harmonics in the resonant *LC* oscillator is negligibly small, therefore the effect of the second harmonic can be taken into account. Thus, to prevent the effect of current source low noise modulation of the second harmonic, it is necessary to provide low impedance for the second harmonic. In other words, it is necessary to create a condition of current source bypassing for the second harmonic. Such an approach to the phase noise improvement is called a filtering technique. Several examples of the filtering technique applied to the differential *LC* oscillators are given in [22].

The simplest circuit solution, which can be applied to the differential tail-biased VCO shown in Figure 20, is to place the shunt capacitance C_s with a large value (resulting in a small reactance at the second harmonic) in parallel to the current source M_1. However, care is required with the large value of shunt capacitance in order to eliminate the self-modulation phenomenon resulting in AM-FM conversion. As an alternative, inserting the series inductance between the current source and the tail creates a high impedance for the second harmonic minimizing its contribution to the signal spectrum. Figure 21 shows the circuit schematic with parallel filter based on the series inductance L_f connected in parallel to the capacitance C_f in addition to the shunt capacitance C_s. This parallel filter resonates on the second harmonic. Its impedance is limited only to the quality factor of inductance. As a result, the inserted inductance and two capacitances comprise a complete noise filter for tail-biased differential *LC* oscillator.

Figure 22 shows the differential top-biased LC oscillator schematic where the current source is connected between the positive voltage supply and center tap of the differential inductor. From the principle of DC operation, both tail-biased and top-biased schematics are identical and the position of the current source can be exchanged. However, in practical implementation, their RF performances are different. For instance, the top-biased VCO is more immune to substrate noise because the current source is placed in an *n*-well, rather than in the substrate [22]. However, from an analysis of the flow directions of even harmonics shown in Figure 20 it can be seen that the top-biased oscillator upconverts less flicker noise into phase noise around the fundamental frequency. This means that the level of the second harmonic flowing through the current source for the top-biased differential VCO is less than for the tail-biased oscillator. To minimize the phase noise, the complete noise filter for the top-biased VCO represents the large shunt capacitance connected in parallel to the current source and the second-

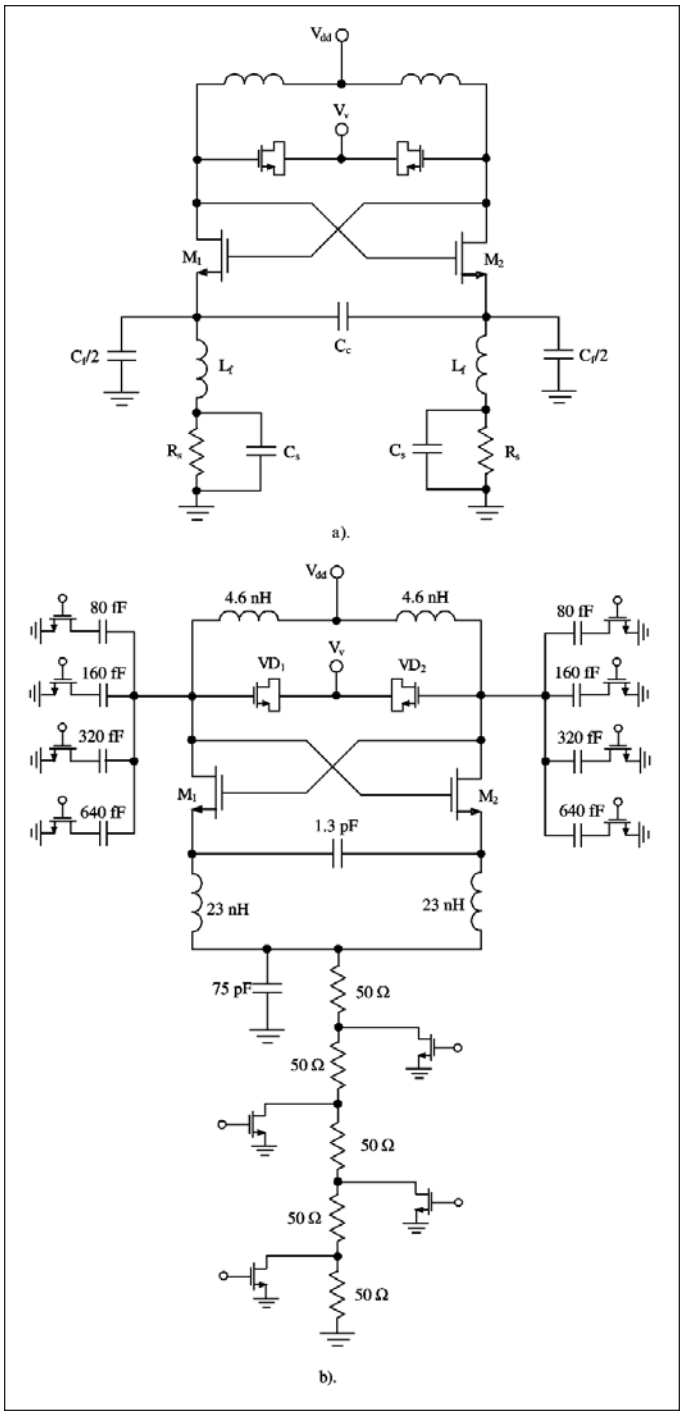

Figure 24 · Differential VCO with noiseless current sources (23).

harmonic filter comprising the parallel inductance L_f and capacitance C_f having high reactance at the second harmonic.

In the extreme operation when it is necessary to increase the VCO output power, a very large gate voltage is applied to the current-source transistor resulting in an almost short circuit to ground for *LC* resonant circuit. This reverts to the voltage-biased differential VCO shown in Figure 23 where a noise filter in the tail is tuned to the second harmonic. In a steady-state operation, this oscillator provides the highest voltage amplitude because there is no voltage drop across the current-source transistor. At the same time, there is no low phase noise upconversion due to the effect of the second harmonic. As a result, the phase noise of the voltage-biased VCO is minimum with the largest amplitude of the oscillation signal.

A tail-biased differential oscillator implemented in 0.35 μm CMOS technology can provide the phase noise of –153 dBc/Hz at 3 MHz offset from the oscillation frequency of 1.2 GHz and consumes 3.7 mA from supply voltage of 2.5 V. The phase noise of the identical reference oscillator without noise filter is 7 dB less at the same offset. A top-biased oscillator using the same technology with tuning oscillation frequency from 1.0 to 1.2 GHz provides the phase noise of –152 dBc/Hz at 3 MHz offset, an 8 dB improvement over its reference oscillator. The noise filter uses a 10 nH on-chip spiral inductance of square form and a 40 pF MIM capacitor [22].

Figure 24(a) shows the equivalent circuit of the tail-biased differential VCO where, instead of FET current source, a polysilicon resistor R_s, which is substantially free from 1/*f* noise, defines a tail current [23]. The resistor value is small enough that it can lower the loaded quality factor of the resonant circuit. Therefore, to provide RF isolation of the resistor from the resonant circuit, a high value of inductance L_f is used in each part. Together with a parallel capacitance $C_f/2$, it can compose a parallel resonant filter tuned to the second harmonic. A large capacitor, C_s, across each resistor shunts wideband resistor noise preventing its upconversion.The decoupling capacitor C_c is used to improve the balanced operation of two *n*MOS devices, M_1 and M_2, where the fundamental frequency voltages at their sources should be exactly out of phase. When this capacitance is too large, the circuit behaves like a conventional differential pair. However, for zero value of capacitance C_c, the oscillator represents the push-pull schematic where, to provide the soft start-up conditions, it is necessary to use large values forf the filter capacitances $C_f/2$, minimizing their reactances at the fundamental frequency.

In the practical differential VCO using 0.35 μm CMOS technology, the dc current is regulated by segmenting a fixed resistor and selectively shorting the segments with digital bits, as shown in Figure 24(b) [23]. The circuit can be tuned from 1.43 to 1.64 GHz with two *n*MOS varactors, VD_1 and VD_2, connected in parallel with a 4-bit binary-switched capacitor array. The oscillator operates at 2.7 V with drain current of 6 mA. The measured phase noise is lower by 20 dB in the flicker noise-dominated area (less than 10 kHz offset) and by 15 dB at 50 kHz offset com-

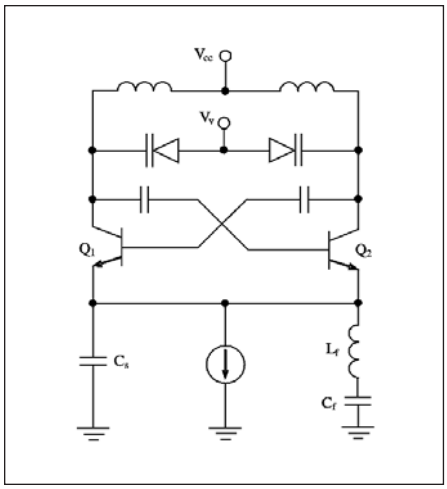

Figure 25 · Differential tail-biased VCO with second harmonic trap.

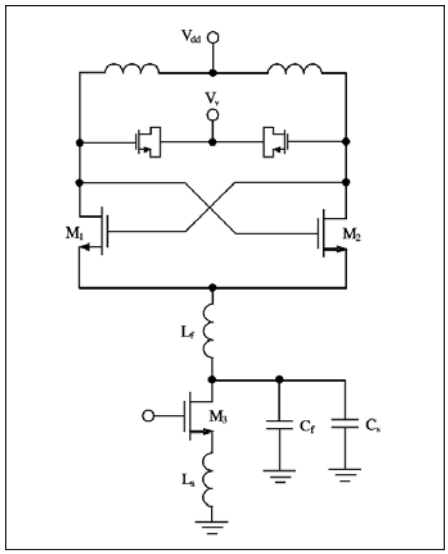

Figure 26 · Differential VCO with tail current noise suppression.

pared with conventional differential VCO. At 1 MHz offset, the phase noise becomes the same for both configurations. Across the entire discrete tuning range, the phase noise changes by only about 2 dB. The degree of suppression is limited by the capacitor C_f, which is determined by interconnects in a practical configuration.

Figure 25 shows the equivalent circuit of the bipolar cross-coupled tail-biased differential VCO where the second harmonic signal generated at the transistor emitters is flowing through the series L_fC_f filter tuned to the second harmonic rather than the current source [24]. The shunt capacitor C_s connected in parallel to the current source suppresses the level of higher-order harmonics, which may appear in the current source. Such a differential VCO configuration is capable to improve the phase noise of –140 dBc/Hz at 3 MHz offset from the oscillation frequency of 900 MHz corresponding to a conventional bipolar differential VCO without second harmonic filter by 1.9 dB.

Figure 26 shows the tail-biased differential VCO using a low noise suppression technique, which includes inductive degeneration and low-pass filtering [25]. An off-chip degeneration inductor L_s is placed between the source of the tail transistor M_3 and ground. In this case, the noise current power of the current source transistor is reduced by the factor of $[1 + jg_m\omega L_s]^2$, where g_m is the transconductance of the transistor M_3. For the values of g_m = 50 mS and L_s = 30 μm, the noise reduction begins at about 100 kHz. The cutoff frequency of the low-pass filter with the series inductance L_f and shunt capacitance C_f can be significantly reduced by using an additional off-chip large value shunt capacitance C_s. The overall phase noise reduction in simulation is 3 dB at the 3 MHz offset from the oscillation frequency of 2 GHz, of which 2 dB are due to the inductive degeneration and 1 dB is due to the on-chip low-pass filter. The supply voltage of 1.4 V and dc current of 9 mA were used, with the off-chip inductance L_s = 100 μm and the following values of the on-chip elements: tank inductor of 2.3 nH with a quality factor of 9 at 2.2 GHz, inductance L_f = 3 nH and capacitance C_f = 10 pF. It should be noted that advantages yielded by the inductive degeneration increase at lower offset frequencies. The practical VCO was fabricated using standard 0.35 μm CMOS technology with

frequency tuning from 1.96 to 2.36 GHz for the same supply voltage and DC current. As it can be easily predicted, the best results are obtained at the highest frequencies when the tuning capability of the varactors becomes the smallest with minimal nonlinearity of their voltage-capacitance characteristic. Using either shunt capacitance C_s = 30 nF or off-chip inductance L_s = 100 μm results in 5 and 6.5 dB phase noise improvement at 3 MHz offset, respectively, compared with the phase noise of a conventional tail-biased differential VCO of –131 dBc/Hz. At 100 kHz offset, the largest contributor to the phase noise reduction is the degeneration inductance L_s providing an improvement from –94 to –103.5 dBc/Hz.

It should be noted that the transistor equivalent circuit parameters like base-emitter capacitance, device transconductance, or collector capacitance, are nonlinear having different nonlinear behavior versus bias voltage. Therefore, there is a possibility to further improve the noise performance by optimizing tail current and resonant circuit elements when the oscillation frequency sensitivity to the tail current is minimized. For example, there is an optimum bias point for MOS transistors where the intermodulation distortions can be minimized due to quadratic dependence of their transfer characteristic in the region close to the device threshold voltage [26]. For bipolar devices, there is a region with medium values of the tail current where the phase noise level of the bipolar VCO can be minimized. Without an emitter degeneration resistor and a low-pass filter, by only optimizing the resonant circuit elements and choosing the optimum tail current of 6.5 mA and power consumption of 14 mW for the 2.6 GHz differential VCO using Si-bipolar process with f_T = 20 GHz, the phase noise level was improved from –92 to –104 dBc/Hz at 100 kHz offset [27].

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