

# Monolithic GaAs Passive Lowpass 3 dB In-Phase Splitter/Combiner

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This article describes the design and performance of a GaAs MMIC splitter/combiner that has a low-pass frequency response and 50 percent bandwidth centered at 2 GHz

The design of an integrated low-pass broadband passive in-phase splitter/combiner is described in this article. The circuit is implemented on a standard GaAs process with three thick metal layers,

high Q capacitors, high Q inductors, nichrome resistors and tightly coupled transformers. The splitter topology consists of a coupled transmission line structure and a 50 ohm to 25 ohm low-pass impedance transforming network. Measurements are presented for an example circuit with 50 percent bandwidth centered at 2 GHz. Across the design bandwidth the insertion loss in excess of the 3 dB power division varies from 1.1 to 1.5 dB, output port isolation is greater than 22 dB, and return loss at all ports is greater than 20 dB. The 2 GHz splitter has a monotonic lowpass response, with 28 dB attenuation at 4 GHz. The absolute amplitude difference between the two output ports is less than 0.1 dB with a variation of a few hundredths of a dB across the passband. The absolute phase difference between the output ports is 0.4 degree, and varies less than 0.1 degree between 1.5 and 2.5 GHz. Die area is smaller than 1 mm<sup>2</sup>.

## Introduction

Recent developments in high Q passive components on GaAs have fostered a new generation of MMICs with fully integrated passive components and interconnects, minimum pin count and 50 ohm ports, as described in the references [1,2]. One consequence of integrating all components and interconnects on

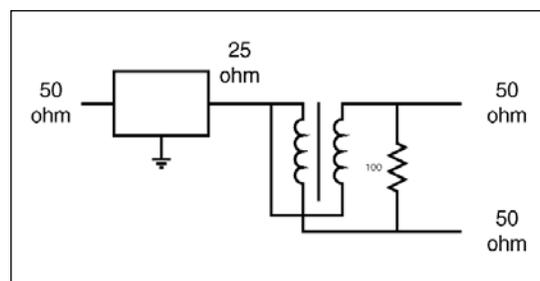


Figure 1 · Basic splitter/combiner topology.

the die is that amplitude and phase errors caused by variations in physical dimensions are reduced by an order of magnitude over discrete passive approaches.

3 dB in-phase splitter/combiners are common passive components and are used in many RF and microwave systems. The splitter/combiner described here was fabricated on TriQuint's TQRLC passive process.

## Circuit Description

The block diagram of a common 3 dB splitter topology is shown in Figure 1. The coupled transmission line transformer offers very low loss to odd-mode currents, while even-mode currents see a large series inductive reactance. Circular and rectangular stacked transmission line transformers are well-behaved when integrated on a low-loss substrate. To match all ports to 50 ohms, an impedance transformer is used between the input and the transmission line transformer.

The 50 ohms to 25 ohms impedance transformer is a low-pass lumped element  $\pi$  network as shown in Figure 2. This network has a few interesting properties, including the fact that constant  $a$  is a free parameter. For opti-

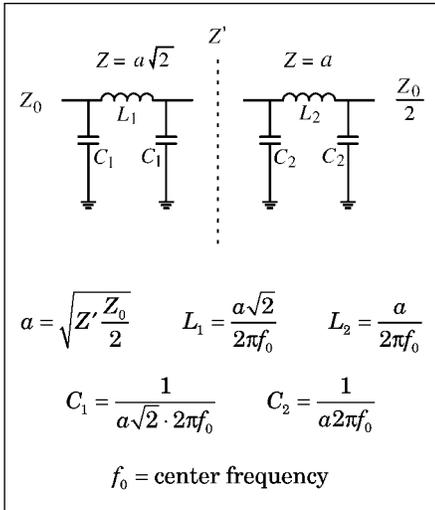


Figure 2 · Impedance transformer design. A smaller  $a$  value requires smaller, lower loss spiral inductors.

imum bandwidth, the intermediate impedance  $Z'$  should be near 35 ohms. However, spiral inductor losses increase with inductance, so network loss may be reduced by selecting a smaller  $a$ . Thus, insertion loss may be traded for bandwidth.

Another consequence of using this 50 ohm to 25 ohm impedance transformer topology is that it also works as a 75 ohm to 37.5 ohm transformer—without changing component values. This splitter topology has very graceful behavior over a wide range of frequencies and termination impedances.

At microwave frequencies, bond

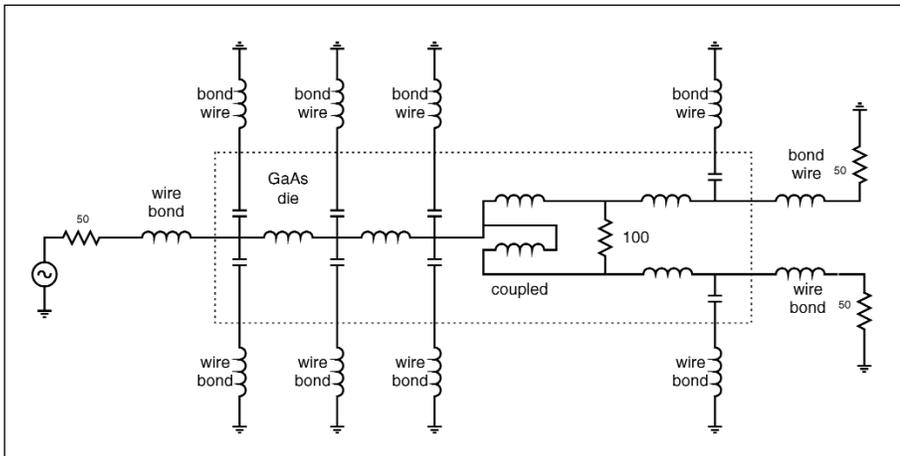


Figure 3 · Complete schematic of the splitter/combiner.

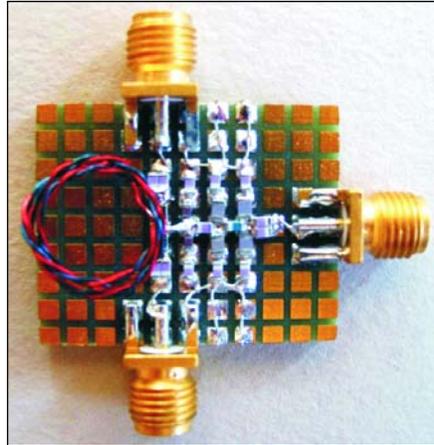


Figure 4 · Layout of the scaled 0.2 GHz circuit.

wire parasitics are significant. Bond wire reactances may be absorbed into network reactances and additional reactive elements added to the output ports, resulting in a practical circuit implementation. The final schematic—which includes the bond wires—is shown in Figure 3.

The unconventional drawing of the ground connections emphasizes the symmetric layout. To verify the design, a  $\times 10$  scaled version at 0.2 GHz was constructed using small chip passive components and an air-core coupled inductor. The scaled circuit is shown in the photo in Figure 4.

### MMIC Design

All element values were calculated from the basic concept using pen-

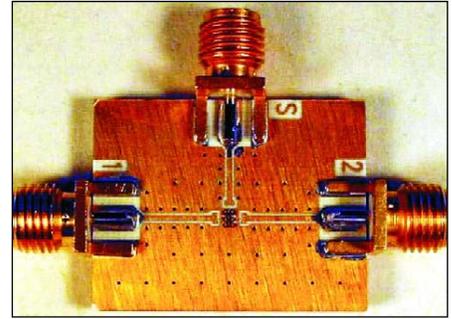


Figure 5 · Splitter die on an evaluation board.

cil and paper and a calculator. The design was then subjected to PSPICE and ADS analysis, and small perturbations were made in element values to compensate for bond wire reactances and imperfect coupling in the transmission line transformer.

When the coupler is connected to equal impedance loads, there are no even mode currents in the coupled transmission lines, so there are no magnetic fields. However, the inductors in the  $\pi$  network carry signal currents. Empty space on the die is used to minimize undesired coupling between the  $\pi$  network inductors and other circuit elements. Figure 5 shows the GaAs die mounted on an evaluation board, and Figure 6 is a die photograph. PSPICE simulations are shown in Figure 7.

### Measurements

Measurements of the 3 dB splitter were made using a Hewlett Packard 8510 network analyzer. A plot of the S parameter magnitudes is shown in Figure 8. Insertion loss is moderate, between 1.1 and 1.5 dB across the

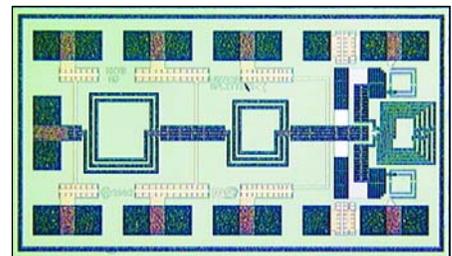


Figure 6 · Die photo of the GaAs splitter/combiner.

GaAs SPLITTER/COMBINER

design bandwidth. Isolation and impedance match on all ports are more than 20 dB across the design bandwidth. The amplitude difference between the two output ports is approximately 0.1 dB, and varies a few hundredths of a dB across the 1.5 to 2.5 GHz design range. The absolute phase difference between the two output ports is 0.4 degrees, and varies less than a tenth of a degree across the 1.5 to 2.5 GHz range. This level of precision is the result of the excellent mechanical tolerances available on the GaAs die.

**Conclusion**

A practical 3 dB in-phase splitter-combiner with good performance has been implemented on a 1 mm<sup>2</sup> GaAs die. Simulation and measurement results are presented for a version centered at 2 GHz. The integrated passive splitter has acceptable insertion loss of 1.1 to 1.5 dB across the design pass band, better than 20 dB return loss on all ports, and more than 20 dB isolation. Output port amplitude and phase match are much better than we have achieved with off-chip passive components in this frequency range, and are consistent with the needs of 40 dB image-reject systems. We would like to thank Mike Doktor for the help in achieving the highly symmetric layouts. The splitter-combiner was fabricated using TriQuint's TQRLC high Q passive process on mechanical grade GaAs.

**References**

1. F. Ellinger and W. Bachtold, "Adaptive Antenna Receiver Module for WLAN at C-Band with Low Power Consumption," *IEEE Microwave and Wireless Components Letters*, volume 12 number 9, September 2002, pp. 348-350.
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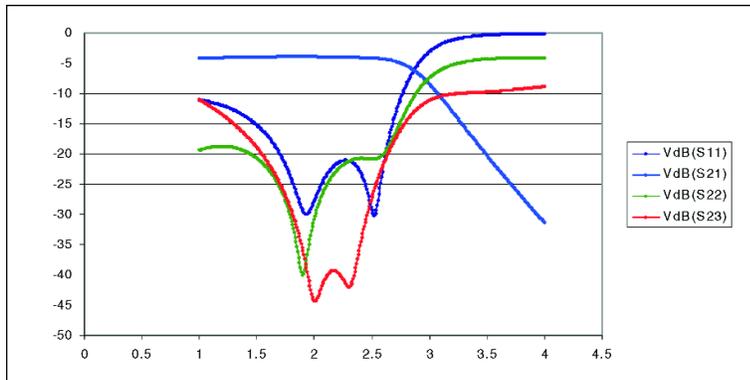


Figure 7 · PSPICE simulation results.

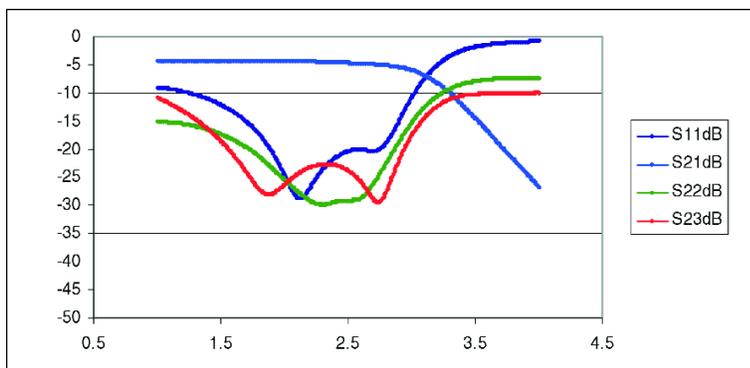


Figure 8 · HP8510 measurement results.

3. Matthei, Jones and Young, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, Artech House 1980, Chapters 6 and 7.
4. Mini-Circuits, *RF/IF Designers Handbook*, Scientific Components, Brooklyn NY 1992, pp. 2-2 to 2-5.

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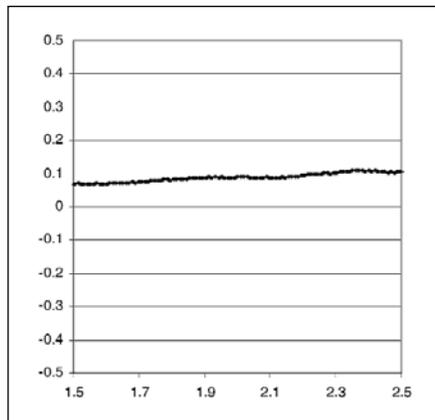


Figure 9 · Plot of S<sub>21</sub> - S<sub>31</sub> amplitude error.

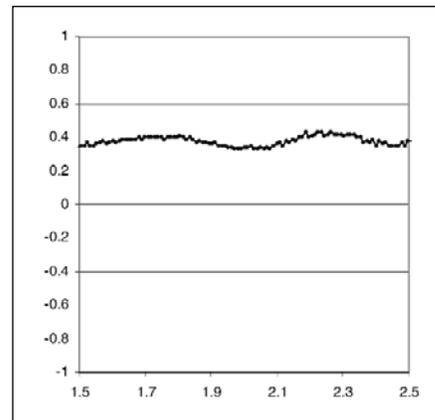


Figure 10 · Plot of S<sub>21</sub> - S<sub>31</sub> phase error.