Data Interface Circuits for PSK Modulators For Data Transmission from Space to Ground

By Jolie. R and D.V. Ramana

In Indian Remote Sensing Satellites, payload data is transmitted from space to ground using a PSK modulator. The PSK modulator may be BPSK, QPSK or 8PSK depending on the volume of data to be transmitted.

In Indian Remote Sensing Satellites, payload data is transmitted from space to ground using a PSK modulator. The PSK modulator may be BPSK, QPSK or 8PSK depending on the volume of data to be transmitted. Different data standards such as TTL, RS-422 and LVDS can be used for transmission of payload data to the modulator on-board the satellite. An interface circuit is required to convert the received data to bipolar levels required for the modulator. This article discusses various interface circuits, hardware realization, and test results.

Introduction

A PSK modulator is used to modulate a high frequency carrier. The carrier frequency should be in the band allotted for data transmission (20 MHz in S-band and 375MHz in X-band), from space to ground. The PSK modulator used is either BPSK or QPSK, depending on the data throughput. In future, it is also envisaged to use an 8-PSK modulator for higher data rate transmission. The payload data from an on-board satellite camera is processed and fed to the modulator. Various logic interfaces such as TTL, RS422 and LVDS can be used. The payload data needs to be converted from the chosen logic level to bipolar levels required to switch the diodes in the modulator.

The data interface circuit for the modulator needs to be designed carefully since the data levels control all the characteristics of the modulator. The main characteristics of a modulator include carrier suppression, phase imbalance and amplitude imbalance. Each characteristic of the modulator is dependent on its drive levels, i.e., the level of data input. The interface circuit can be tuned to get optimized modulator performance. The number of streams of data depends on the PSK modulation scheme used.

In this paper, various modulator data interface circuits such as TTL, RS-422 and LVDS, which are used in Indian Remote Sensing Satellites, are discussed.

Transistor-Transistor Logic (TTL) Interface Circuit

For many years, TTL logic has been used for data transfer between the on-board data processing circuits and the RF modulator. The TTL logic family is relatively slow compared to many of the fast switching logic families available today. However, it was used recently in satellite applications where the data rate is 52.5 Mbps per stream. The total data rate transmitted using QPSK modulation is 105Mbps.

A TTL driver circuit for the modulator, designed and realized for space applications, is shown in Fig.1. The TTL logic levels are 0V and 5V. Initially, the data transmission rate was 5.2Mbps and TTL interface was used for a BPSK modulator. As the volume of payload data increased, the data transmission rates using TTL have been set to as high as 52.5Mbps per channel and QPSK modulation is used.

Three RG316/U cables (for I-data, Q-data and Clock) are used for data transmission
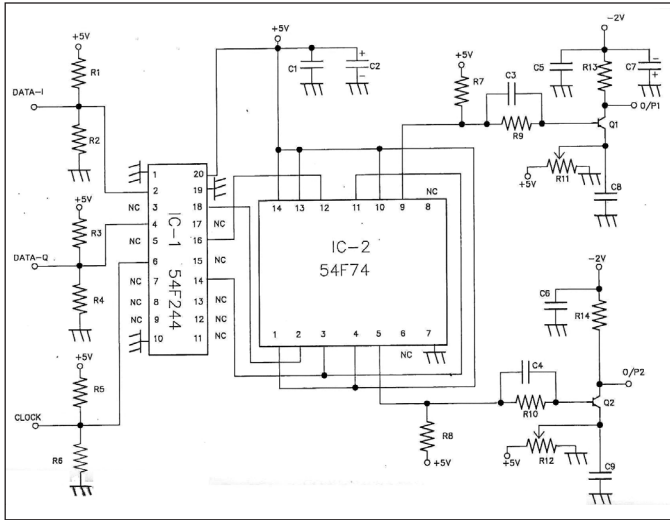
Figure 1 • TTL driver circuit

between the data processing package and the RF modulator package. The data processing and modulator packages are mounted at different locations on the satellite panels and the length of the cables carrying 52.5Mbps data is of the order of 3.9m each. As the data passes through lengthy cables, it is observed that the data quality degrades in terms of rise/fall time and duty cycle. This is due to parasitic capacitance in the long length of cables. The data quality is regenerated by passing through a buffer.

The TTL driver circuit consists of a buffer (54F244), D-flip flop (54F74), switching transistors (NE 88908) and passive components. The high speed buffer (54F244) is used at both the transmitting and receiving ends of the data transmission cables. The buffered I-data, Q-data and Clock are fed to a latch 54F74 IC. Here, the clock is used to synchronize the two data streams so that both appear at the modulator at the same time. The latched I and Q data are fed to switching transistors to convert them to bipolar levels required for biasing the PIN diodes in the reflection type modulator. The potentiometers in the circuit are fine-tuned to achieve the appropriate bias levels required for the modulator to meet its specifications of carrier suppression, amplitude imbalance, and phase imbalance. The
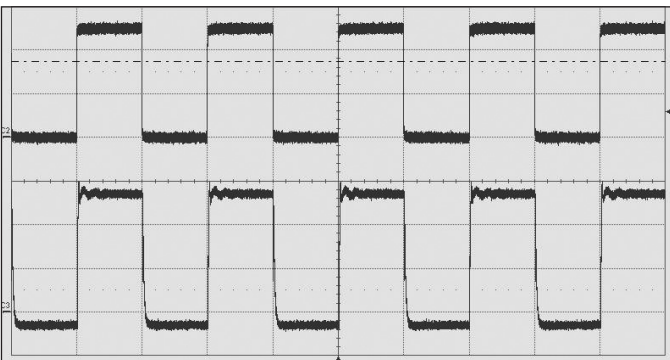

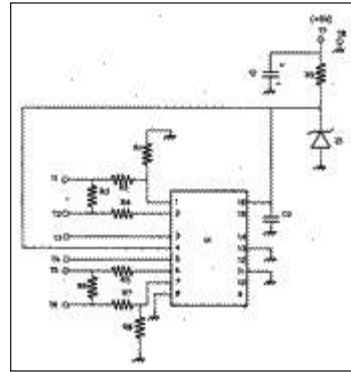**Figure 2 • Input and output of TTL data interface circuit**

input and output waveforms of the TTL data interface circuit are shown in Fig.2.

RS 422 Interface Circuit

Another logic interface used for data transfer onboard the satellite was RS422. A modulator interface circuit was developed to accept the RS422 levels.

Figure 3 • RS422 Line Receiver circuit

The RS-422 is a differential, or balanced, signaling technique. A termination resistance of 100Ω is required at the input of the 422 receiver. The RS422 offers a maximum prescribed common mode voltage range of -7V to +7V, which helps to counter transient spikes and ground shifts.

A twisted pair shielded cable is used for data transmission between the payload and the RF modulator package. At the transmitter end, 26LV31 IC is used. The interface circuit consists of a line receiver and level converter. The line receiver (26LV32) shown in Fig.3 converts RS422 levels to TTL levels. The data is converted to bipolar levels using the level converter shown in Fig.4. The potentiometers are tuned to get bipolar levels which are suitable for biasing the modulator. The differential inputs and the bipolar output of the RS422 data interface circuit is shown in Fig.5.
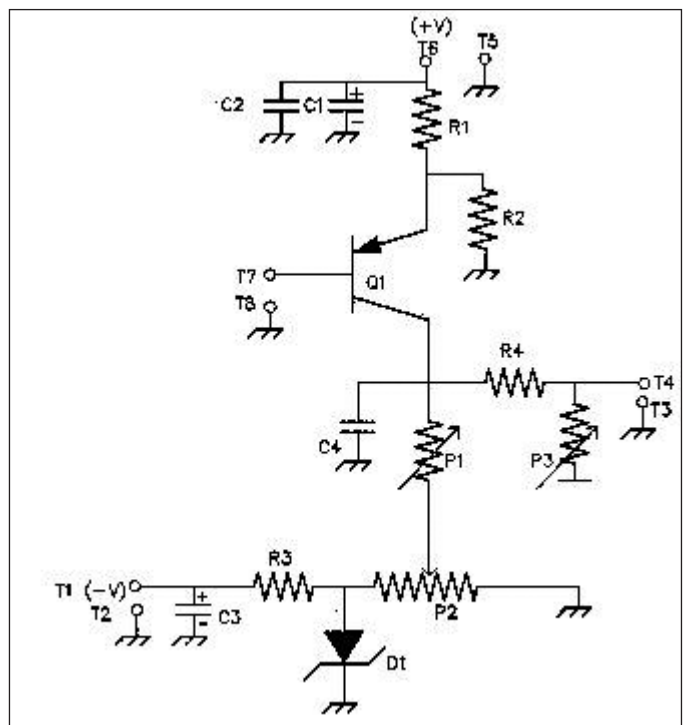

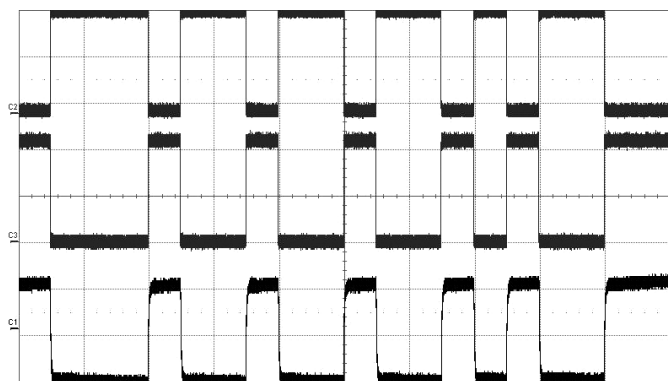**Figure 4 • Level converter in the RS422 driver interface circuit**

Figure 5 • Differential inputs and output of RS422 interface circuit

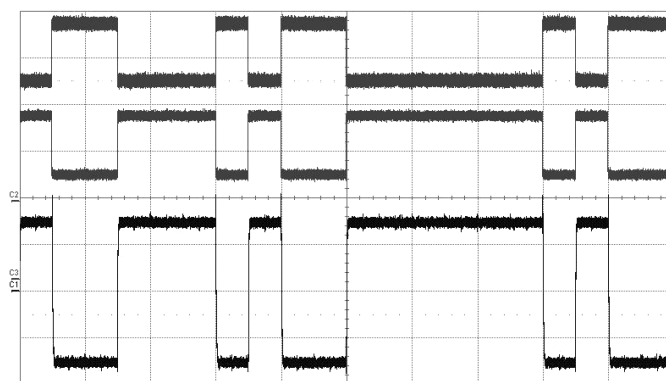## Low Voltage Differential Signaling (LVDS) Interface Circuit

The latest interface level currently being used on-board satellite is Low Voltage Differential Signaling (LVDS). An LVDS transmitter (90LV31) converts the processed data into a low voltage differential signal. This is received at the modulator input through twisted pair differential cable. The data interface circuit shown in Fig.6 consists of an LVDS receiver (90LV32) that translates the differential signal into a TTL/CMOS signal. The LVDS receiver has simple termination requirements – usually one resistor at the input of the receiver compared to multiple resistor solutions for other standards. The characteristic impedance of the PCB trace or cable should match with the termination resistor of 100Ω which in turn should be placed as close as possible to the input of the receiver. A 100Ω twisted pair differential cable is used to carry data from the data processing circuits to the modulator.

The output of the LVDS receiver is fed to a latch (54F74) for latching the I and Q data with respect to the clock. This is required to synchronize both the data streams. The clock input to the circuit and the latch can be avoided provided exact length of cables is maintained between the LVDS transmitter and receiver. Also, there should be no skew between the differential pair of lines on the PCB. The latch is followed by a level converter circuit.
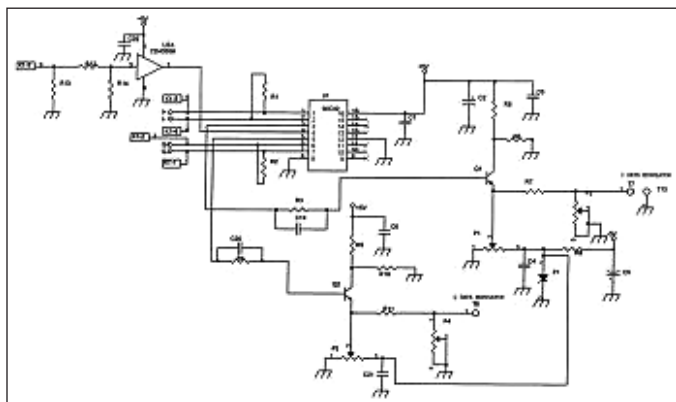

Figure 6 • LVDS driver interface circuit

Figure 7 • Differential inputs and output of LVDS driver interface circuit

Potentiometers in the circuit are used to provide suitable bias levels to the modulator. The differential inputs and the output of the LVDS driver interface circuit are shown in Fig.7.

Conclusion

This article discusses various data interface circuits which are practically realized for PSK-based payload data transmission from space to ground. The modulator requires an interface circuit to convert data from different logic levels to the bipolar levels. Data interface circuits such as TTL, RS422 and LVDS are discussed and hardware test results are presented.

About the Authors

Jolie.R received her B.Tech from University of Kerala and M.Tech from Cochin University of Science and Technology. She joined ISRO Satellite Centre, Bangalore in 2000 and is a design engineer for data transmitting systems for IRS satellites. Her work includes development of high bit rate modulators, data transmitters at X and Ka-band and investigations into spectrally efficient data transmission systems for space communication links. She is currently registered for a PhD (part time) at VTU, Bangalore. jolier@isac.gov.in.

Dr. D. Venkata Ramana holds an M.Tech degree from National Institute of Technology, Surathkal and a Ph.D from Indian Institute of Science, Bangalore, India. He joined ISRO Satellite Centre, Bangalore in 1983 and has been associated with the Communication Systems Group. He is involved in the design and development of high bit rate data transmitters and advanced modulation schemes for various Indian Remote Sensing Satellites. He currently heads a Ka-band data transmitter development team for satellite applications. He has published papers in various national and international journals. He is a Senior Member-IEEE, Fellow-IETE, Fellow-IE, LM-IMAPS. dvramana@isac.gov.in.