

Productivity by Design: ADS 2008 Reduces Steps to Simulation and Verification

How-Siang Yap
Agilent EEsof EDA

The latest update to this well-known EDA system includes usability enhancements that can greatly reduce the time and effort required to create and analyze new designs

In today's challenging environment for RF, high-speed communications product design, development cycles must shrink if profits are to grow. Circuit designs that meet the latest specifications must get to the

marketplace ahead of the competition to ensure the success of the design group creating them, and margin for error is slight or non-existent.

Agilent EEsof EDA, the electronic design automation division of Agilent Technologies, has a more than two-decade history working with key customers to develop advanced RF-mixed signal simulation technologies for optimal performance and yield in RF-mixed signal and high speed products. The latest release of its Advanced Design System (ADS) is the first in a series of four releases in 2008 designed specifically to double productivity for common design tasks over previous ADS versions.

ADS 2008 adds easier access to the powerful simulators the software is known for, largely through enhancing the graphical user interface (GUI). With this new release, the underlying ADS 2008 user interface uses the same advanced GUI development platform for the latest internet applications, such as Google™ Earth, to enable quick implementation of capabilities for enhancing user productivity and development speed throughout the design flow.

This article discusses the considerations for using ADS 2008 to double designer productivity when performing common design and development tasks.

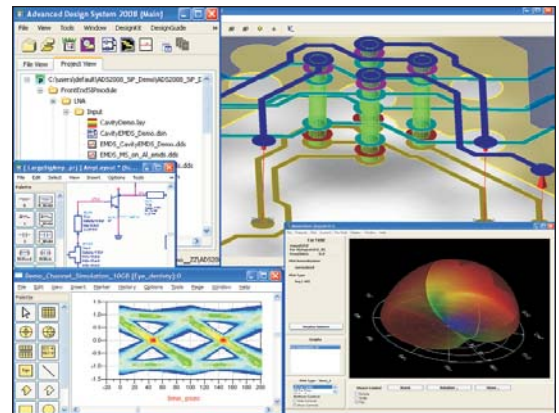


Figure 1 · Advanced Design System 2008 doubles productivity by adding easier access to powerful RF-mixed signal and 3D EM simulators.

Productivity improvements are measured in terms of reducing the following:

- Activities needed to accomplish a particular design task
- Number of mouse clicks
- Simulation time

A sample listing of these improvements is available through the following link: http://eesof.tm.agilent.com/products/ads2008_productivity.html.

Design Navigation

By far the most routine design tasks include navigation and steps to:

- Prepare schematics for simulation
- Lay out the design to prepare it for electromagnetic simulation and fabrication

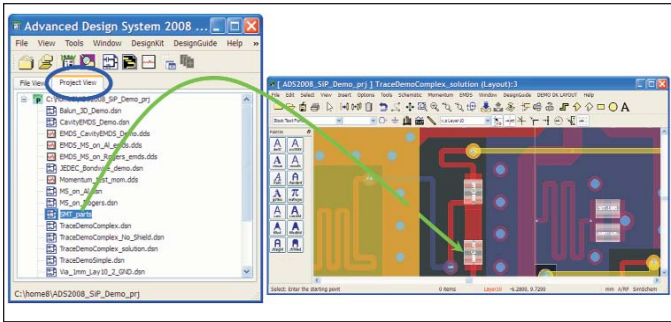


Figure 2 · Existing designs can be reused by single step drag-and-drop action without needing menu picks.

Reducing the number, or simplifying navigation of menu picks and mouse clicks can save significant time, which is better spent in design creation and assessment.

For example, zooming in and out is now accomplished by scrolling the mouse wheel instead of taking the eye off the design to pick the zoom menu. Panning across the design also does not require the user to take the eye off the design to drag the horizontal or vertical window edge pan bars. It is done simply by holding down the right mouse button to pan in any direction instantly.

Project Management

Reusing designs from multiple exiting projects is a common task that involves:

- Copying and renaming new versions of the design to start work on
- Collecting and organizing the designs into intuitive folders and hierarchies
- Inserting and combining existing designs into the current one

ADS2008 now accomplishes these tasks through single-step copy and automatic renaming of hierarchical designs into intuitive, user-defined project view folders. Existing designs can be dragged and dropped into new ones, without the need for menu picks.

Multi-Layer High-Frequency Physical Design

High frequency physical designs are increasingly multi-layer for RF modules, System-In-Package (SIP), RF boards and MMIC. Drawing these structures correctly for electromagnetic (EM) simulation or hardware fabrication is a significant part of the design and contains many sub-tasks, including:

- Drawing, alignment, and connection of vias, traces, interconnects and bond wires across multiple layers.
- Verifying layout against schematic design.
- Verifying layout against design rules.

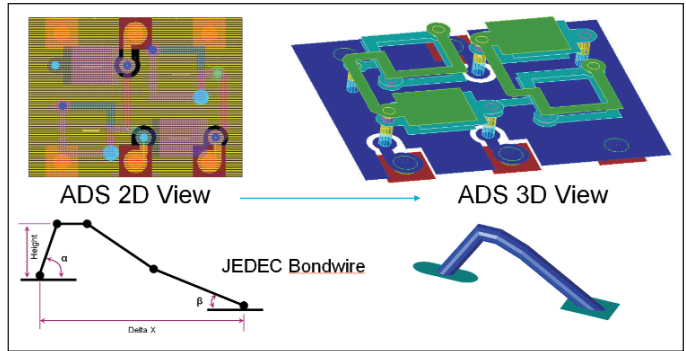


Figure 3a · 3D viewer allows easier visualization of multi-layer layout and bond wires than 2D views.

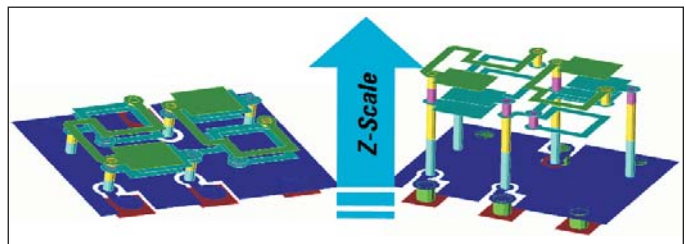


Figure 3b · Vertical stretching allows via connections to be inspected interactively.

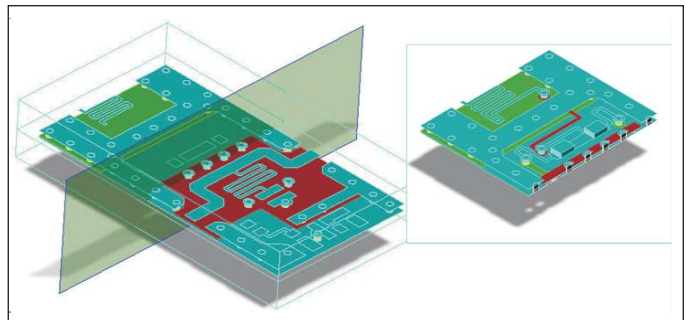


Figure 3c · Sliding 3D cut-planes through a complex multilayer design provide interactive cross sectional views to inspect proper interconnections.

- Verifying layout manufacturing output against original layout design.

ADS2008 now enables automatic via insertion during multi-layer trace routing with hot-key traversal through layers. This allows a complete multi-layer interconnect to be inserted in a smooth, continuous sequence without multiple distracting menu picks of layers, traces, and vias. JEDEC-compliant profile of bond wires can be directly drawn in layout to connect traces to packages for subsequent EM simulation.

All layers can be simultaneously viewed either through 2D-translucency or 3D interactive viewing to verify cor-

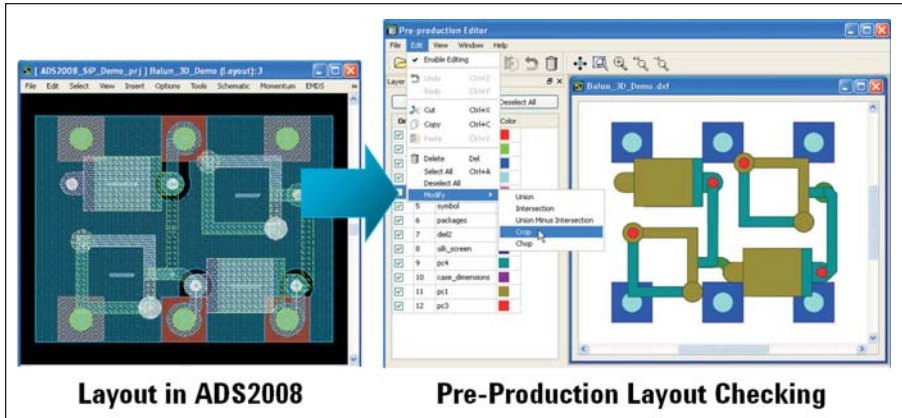


Figure 4 · Pre-Production editor verifies manufacturing layout file output against original layout design in ADS2008.

rectness. The 3D viewer also enables interactive vertical stretching and sliding cut planes to examine the proper interconnection of vias, traces, and bond wires within multilayer structures.

Design synchronization between layout and schematic provides interactive layout-versus-schematic (LVS) verification as the layout design progresses. The designer has full control over the layout process by switching between auto or manual design synchronization as needed for achieving speed with precision placement.

Design rule checking (DRC) reports all violations in a scrollable list with auto-zooming of the selected error on the layout to quickly guide the user to fix the error location.

The layout output file such as DXF or Gerber for manufacturing is verified for correctness against the original layout design via a pre-production editor, which also allows

additional manufacturing required adjustments such as cropping or union of layer information.

Simulation Integration Productivity

EDA tools allow quick exploration of multiple design possibilities through simulation. However, multiple simulation technologies are needed to provide more complete answers to make the best design decisions. For example, full 3D and planar 3D EM simulation are needed to examine the impact of bond wires, packaging, finite dielectrics, and ground planes on circuit performance. Considerable time is saved when system, circuit, and EM simulators are integrated into the design environment to use the same set of design data input for separate simulations or combined co-simulation and co-optimization. This eliminates unproductive, error-prone manual design

data translation and re-entry with standalone EM simulators.

ADS 2008 integrates full 3D EM using finite element method (FEM) analysis with the convenience of re-using the same physical design data input from its layout environment and planar 3D Momentum EM simulator without manual design re-entry. This makes the full power of system-circuit-EM co-simulation or co-optimization available to the designer for thorough design exploration without leaving the design environment

Speeding Up Simulation

As designs become larger due to increased integration complexity, the capabilities of simulation algorithms to accommodate capacity with convergence and speed must keep pace. The quality of available simulation engines can vary significantly when compared with one another. Therefore, designers cannot assume that all harmonic balance simulators are equal simply because they share the same analysis technique.

Another current trend is the affordable availability of powerful 64-bit multi-core and multi-node parallel computing resources that simulators can take advantage of. Particularly, EM simulations that traditionally consume the most computing time and power can now benefit from parallel computing to return design exploration data fast enough for EM to become increasingly a design tool instead of a sign-off verification tool.

ADS 2008 has improved simulation speed, capacity and convergence in multiple areas to make faster computations available to the designer. In DC, AC, and transient simulation, the algorithm has been refined to increase simulation speed by an average of 6x for large designs containing over 10,000 nodes. In addition, 64-bit data structure enables much larger design simulation data to be collected, processed and viewed. Multiple convergence techniques are employed

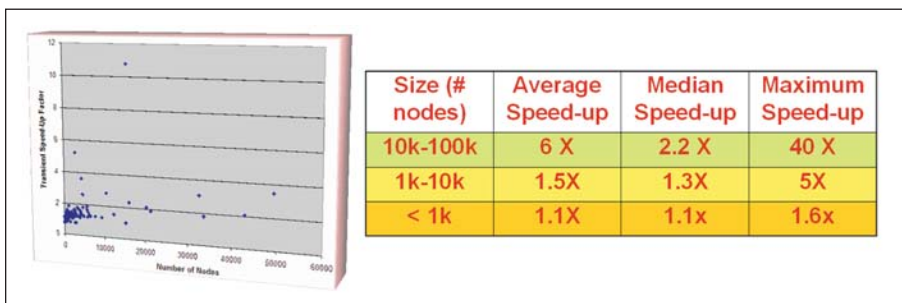


Figure 5 · ADS 2008 improves DC, AC and Transient simulation speed for large designs by over 6x.

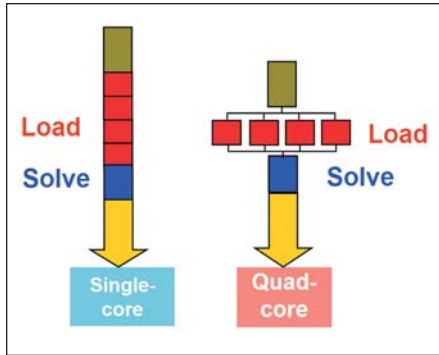


Figure 6 · By taking advantage of multi-core processors, 3D planar EM simulation is now sped up by 100% for larger problems by parallelizing the matrix load solution process across the processor cores.

in unison such as using transient simulation to find starting conditions for highly non-linear harmonic balance or circuit envelope simulations

Momentum, the planar 3D simulator in ADS 2008, now takes advantage of multi-core processors for parallel matrix-loading. This technique improves simulation speeds by more than 100 percent for large designs.

A new optimization technique, called simulated annealing, improves optimization convergence in problems where the optimized variables vary over a very wide range where multiple local minima exist to trap more traditional gradient, random or hybrid optimizers.

ADS 2008 also is HSPICE netlist compatible, meaning that external designs captured as an unencrypted HSPICE netlist can be simulated directly in ADS without time-consuming manual translation. This is especially useful for high-speed serial link signal integrity designers who get the models of their input and output buffers in HSPICE format from digital IC suppliers.

Instant Productivity Assistance

Designers often have little time to learn how to use the new capabilities of the latest EDA tools even though the benefits of significant productivi-

ty gains exist. Since this is a common trait among designers, the EDA tool provider is faced with opposing requirements—to make more powerful simulations available while also making them easier to access, learn, and use.

ADS 2008 has completely redesigned its Help rendering system to enable quick access through a single click from any Help page. The Help menu contains hyperlinks to:

- Instructional videos of common design tasks
- The Agilent EEsof EDA knowledge center
- Design examples
- Documentation

Designers who are accustomed to using previous versions of ADS can still continue to operate ADS 2008 in the same way while they learn the new productivity enhancing capabili-

ties described in this article

Summary

Advanced Design System 2008 from Agilent EEsof EDA represents significant enhancements to deliver 100% productivity improvements over previous versions of ADS through improvements in user interface, simulation algorithms, and integration and support for parallel computing resources. Planned update releases this year will further deliver on productivity by design.

Author Information

How-Siang Yap is a Product Manager at Agilent EEsof EDA. He can be reached by e-mail at: how-siang_yap@agilent.com

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http://eesof.tm.agilent.com/products/ads2008_productivity.html
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