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Design Issues With High Speed Digital Interconnections

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This tutorial gives inexperienced engineers an idea of the types of design difficulties they might find with high speed interconnections at the device, board and system levels

Even the most experienced engineers struggle to find an efficient means of designing high performance interconnections in their high speed digital design projects. Maintaining good signal integrity for reliable high speed information transfer is perhaps today's most-studied subject in this area of design engineering, at all levels from device-to-device connections, board-to-board connections, or connections between the various pieces of equipment that make up a complete system.

This tutorial is intended to be a reminder of the primary issues in high speed interconnections at the device level, the board level and at the system level, including connection to test instrumentation.

Device-Level Interconnections

Within an integrated circuit or multi-chip device, interconnections are made using semiconductor processing techniques. Although a design engineer using that IC may have no involvement in its design, the problem of routing high speed signals has commonality at all levels.

An IC has the advantage of shorter paths, so crosstalk and radiation (dispersion) are less of a problem than at the board level. However, there are many constraints on how those interconnections are made: conductivity of the metal layers, the separation of conductors from ground, allowable routing paths, etc.

Perhaps the greatest issue is maintaining performance from the chip to the package pins that connect to the rest of the circuitry. There still may be different engineers designing the chip—using semiconductor process design software tools—and managing its packaging, perhaps using a microwave type electromagnetics (EM) software package for modeling and analysis of the package.

Board-Level Interconnections

Now that we have reached the edge of the chip, the connection to the board is the next pathway to consider. Most high speed devices use a ball grid array (BGA), with the necessary number and size (pitch) of connections to support the function of the device.

Much research in both industry and universities has been devoted to the analysis of the connection between packaged chip and the printed wiring board (PWB). The primary tool is EM analysis, which may also be used to develop models of the interconnects that can be used in EDA simulation of the entire circuit. Of course, the mechanical properties of the interconnect must be consistent, so additional research effort has been applied to the methods of assembly.

The next portion of the signal path is currently the most researched and analyzed part: the routing of signals on the PWB. Reliable high speed performance can only be achieved with a well-designed board that is fabricated and assembled accurately and consistently.

The etched copper traces that carry the digital signals are the first step. Designers must consider whether a single conductor is appropriate, akin to a microstrip line for microwave circuits. Perhaps control of crosstalk requires the line to be routed between nearly solid shielding layers of the

PWB, as with stripline microwave circuits. Or, for highest performance, balanced lines may be required to maintain signal integrity performance in the presence of an inconsistent ground plane, or to minimize ground currents that can add losses or distort the signal propagation along the lines. This is similar to the use of coplanar waveguide and balanced, ground-independent circuits in microwave devices.

One major difference between digital PWBs and microwave circuits is the number of signal, control, and clock lines that are required in a digital system. PWBs for high performance digital systems may have 8, 12 or even 24 layers, which makes one design feature exceptionally critical—the *via*.

Microwave engineers will recognize that a via is a discontinuity that can create reflections, alter impedance and add dispersion loss to the circuit. All of these things are equally damaging to digital signals, where alterations to the timing, voltage level and edge rates can greatly impair the circuit's ability to reliably carry the signal. These effects, collectively referred to as *signal integrity*, are currently the subject of intense study. While signal lines are certainly part of the signal path, vias are unquestionably the single most important feature requiring attention.

Figure 1 provides an idea of the complexity of the circuit behaviors that surround a via. The various parasitic capacitances and inductances make this a complex structure to analyze. In addition, EM analysis (not shown) will reveal effects at the line-to-via junction, between the via and the copper layers it passes through, and again when it transitions to another line. These points will create inconsistencies in current density that will reduce performance unless the designer is able to minimize their effects by precise design of the mechanical structure to compensate for the variations.

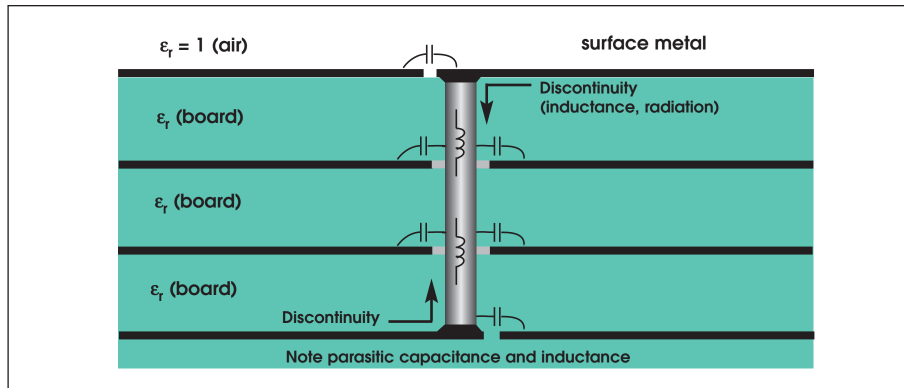

Figure 1 · Diagram of a via, showing the major areas of behavior that make it a complex structure for modeling and analysis.

System-Level Interconnects

Board-to-board connectors are another area of significant design effort. The modular nature of modern computing equipment requires these interconnections, but like vias, they represent potential large disturbances to the signal as it propagates through the system.

Some connector manufacturers have undertaken analysis of their connectors and the connection to the PWB. A few have developed design rules or a recommended reference design for the PWB metal in the vicinity of the connector (e.g., Samtec's "Final Inch"). This can simplify the engineer's task.

Cabling is an even greater challenge, with the same issues of connecting to the board, but with the added requirement of maintaining performance on a multiconductor, shielded, flexible cable. The cable must maintain consistent electrical performance up to tens of GHz bandwidth in some cases.

Test instruments are the typical applications for cables of significant length. A few test applications have required an interface that is embedded in the digital circuit, to avoid problems with the cable length, which may also have excessive loss. The difficulty of high speed test connection means that end-to-end testing is still the primary means of system performance evaluation.

Simulation and Modeling

Trial-and-error is much too time consuming and expensive for high speed digital device and PWB design, so designers rely heavily on computer simulation. However, as bus speeds increase, the difficulty of modeling also increases. Electromagnetic analysis is usually required for accurate simulation of signal behavior, but as Figure 1 illustrates, the complexity of the structure creates a very large problem to be analyzed. Reports of a multilayer PWB requiring two days of computation time for a single pass of EM analysis are not unusual. At this time, EM tools are used to analyze portions of the structure that are repeated, and a simplified model of those elements is used to achieve faster simulation times.

Complete and highly accurate modeling and simulation of high speed PWBs is still in the future, although the current simplified EM models, along with circuit theory-based models, can provide acceptable results at today's performance levels.

Simulation is another area of intense research effort. Two specific topics are vias and classic microwave EM analysis of transmission lines. These two areas cover the primary portions of the digital signal path on a PWB. Vias are especially important because of their commonality in multilayer boards, as well as the complexity of their structures. A number

of companies have addresses specific aspects of via design and performance in their EDA software offerings.

Future Possibilities

Continued work on computer modeling and simulation is essential for the support of future generations of digital circuits that operate at even high speeds. Given the number and scope of current research efforts, we can expect steady improvement in the ability of EDA tools to assist engineers in the design of high performance boards.

Another are of research involves the elimination of large portions of the digital signal path. There have been several proposed methods of integrating optical communications onto digital ICs. Then, optical links will carry the high speed signals among the various devices that make up the system. Among the concerns raised for such systems are reliability of separate interconnecting cabling (instead of proven PWB technology), and power consumption of the high speed optical devices. New technologies are being developed to address these issues, but this solution appears to be a relatively distant future possibility.

More effort to contain the high speed operations on a single device—without requiring transfers to other devices—is another area of research. This also seems to be further into the future, since new memory technologies need to be refined, and smaller-feature IC fabrication will be required to place additional functions onto a chip instead of distributed around a PWB.

Summary

High speed digital interconnections is a active, and important area of design. And it is a key engineering area where there is significant sharing of expertise among digital and microwave engineers, with a positive impact on the results.

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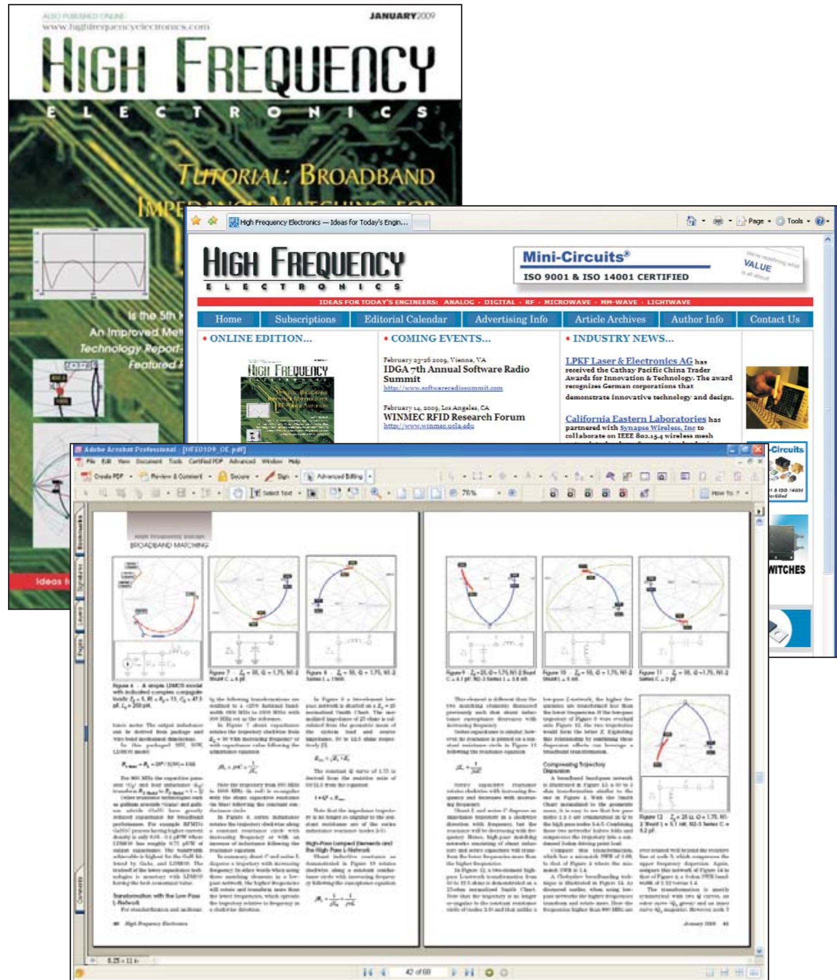

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