

A Design Tool for Improving the Input Match of Low Noise Amplifiers

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This article describes the mathematical basis for tradeoffs among noise figure, gain and return loss of an LNA, with implementation in an EDA design tool

This article will describe the methods and mechanisms for trading excess output return loss for improved input return loss while maintaining low noise figure (NF) in a

low noise amplifier (LNA) design. Other methods for improving LNA input match, such as trading noise match for input match or employing series negative feedback [1], sacrifice gain in the process. While gain reduction may also be the result of trading output match for input match, there is an opportunity for maintaining approximately constant gain during this process, since matching gain lost at the output can be recovered by the improvement in input match.

Figure 1 is constructed to clarify the meaning of many of the important design parameters. These are impedances or reflection coefficients as seen by looking in either direction across the device (input and output) interface planes. Impedance (Z) and reflection coefficient (Γ) are shown for both directions at each plane. Z and Γ are related to each other through a given reference impedance (Z_R) according to the formulas in [2, 3]:

$$\begin{aligned}\Gamma &= (Z - Z_R^*)/(Z + Z_R) \\ &= (Z - Z_0)/(Z + Z_0) \text{ for } Z_R = Z_0 \text{ (real)}\end{aligned}\quad (1)$$

$$Z = Z_0(1 + \Gamma)/(1 - \Gamma) \quad (2)$$

In keeping with the notation of much of the literature on the subject, Z_S refers to the transformed source impedance (not the generator impedance). This is the impedance that

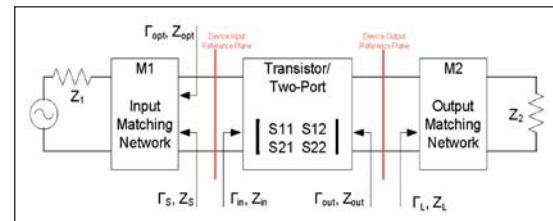


Figure 1 · Low noise amplifier (LNA).

the transistor sees looking into the input matching network. Z_L is the transformed load impedance that the transistor sees looking into the output matching network (not the load impedance terminating the amplifier's output port). Z_{in} and Z_{out} refer to the input and output impedances of the device/transistor (not the impedances at the input and output ports of the amplifier). Z_1 and Z_2 in Figure 1 represent the generator and load impedances and are usually both Z_0 ($Z_1 = Z_2 = Z_0$).

Designing an amplifier for maximum gain (G_{max}) at a given frequency requires the calculation of a unique pair of termination impedances that will provide a simultaneous conjugate match at both ports and yield the maximum gain for the device/transistor used (provided that the device is unconditionally stable at the given frequency). The required terminations can be calculated from the S -parameters of the device [3]. Likewise, a unique pair of termination impedances determine the minimum noise figure and maximum associated gain of the amplifier. However, in this case, noise parameters for the device are needed in addition to the device's S -parameters.

In both of these design scenarios, there is no flexibility in the choice of termination

LNA INPUT MATCH

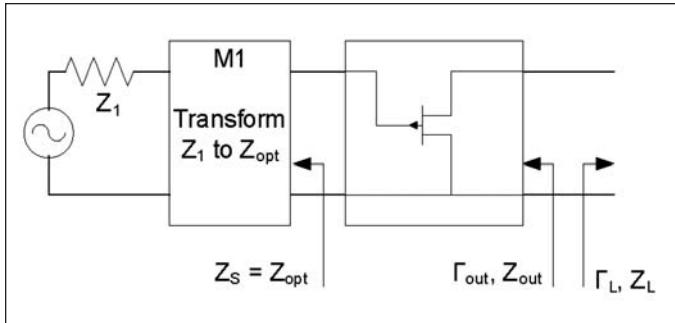


Figure 2 . Select the input impedance and determine the output impedance.

impedances because the solution set is represented by just two points on the Smith chart. If a compromise can be made in either the gain or noise figure (or both) then the solution set of termination impedances for a given gain and noise figure immediately becomes infinite as represented by circles in the Smith chart instead of just two points. This article will describe how excess output return loss can be traded for improved input return loss while maintaining the noise figure near the optimum value (F_{\min}) for the amplifier. The mathematical solution is quite involved and the graphical solution (on a Smith chart) can be tedious. The LINC2 program from Applied Computational Sciences completely automates this process, as will be shown toward the end of this article.

The Noise Figure as a Function of Z_S

The noise figure of a linear two-port amplifier can be formulated as a function of only four parameters:

- 1) F_{\min} , the minimum noise figure of the device/transistor
- 2) Γ_{opt} , the optimum source reflection coefficient for achieving F_{\min}
- 3) R_n , the device noise resistance
- 4) Z_S , the actual source impedance applied to the input of the device

The noise figure, F , is then calculated according to the following formula [3]:

$$F = F_{\min} + (r_n/g_s) |Y_S - Y_O|^2 \quad (3)$$

where F_{\min} is the minimum noise figure, r_n is the normalized noise resistance ($r_n = R_n/Z_0$), Y_S is the source admittance ($Y_S = g_s + jb_s = 1/Z_S$), and Y_O is the optimum source admittance ($Y_O = g_o + jb_o = 1/Z_{\text{opt}}$).

Three of the four parameters in Equation 3 are fixed constants that are determined by the device characteristics at a given frequency. It is interesting to note that, apart from the device constants that cannot be changed

by the circuit designer, the noise figure for the amplifier is completely determined by the source impedance Z_S . Since the noise figure is a function of only one variable, the circuit designer has only to select a Z_S value that gives the desired noise figure. Only one value of Z_S ($Z_S = Z_{\text{opt}}$) gives the minimum noise figure F_{\min} . Other values of Z_S yield larger noise figures and the solution set for any noise figure larger than F_{\min} is represented by a circle (called a noise circle) on the Smith chart. Many simulation programs, including LINC2, have the ability to plot these noise figure circles as an aid in selecting the source impedance that will yield the desired noise figure.

Designing for Minimum Noise and Maximum Associated Gain

A common approach used in the design of RF low noise amplifiers is to design an input matching network that will transform the source impedance from 50 ohms to the optimum value for minimum noise (determined by Γ_{opt}) and then terminate the output with a conjugate match. This is easy to do since we can apply $\Gamma_S = \Gamma_{\text{opt}}$ at the input terminals of the device and calculate the required load reflection coefficient $\Gamma_L = \Gamma_{\text{out}}^*$ for the conjugate output match. A circuit simulation can be run on the circuit shown in Figure 2 to determine the output impedance (Z_{out} from Γ_{out}) with Γ_{opt} as the source termination, or the following formula can be used to calculate this impedance directly.

$$\begin{aligned} \Gamma_L &= \Gamma_{\text{out}}^* = (S_{22} + S_{12} S_{21} \Gamma_S / (1 - S_{11} \Gamma_S))^* \\ &= (S_{22} + S_{12} S_{21} \Gamma_{\text{opt}} / (1 - S_{11} \Gamma_{\text{opt}}))^* \end{aligned} \quad (4)$$

$$Z_L = Z_0 (1 + \Gamma_L) / (1 - \Gamma_L) \quad (5)$$

At this point we have all the necessary information to design the low noise amplifier. Matching networks are designed to transform Z_0 to Z_{opt} and Z_L at the input and output terminals of the device respectively. To complete the circuit, bias networks are designed to feed the supply voltages to the device.

The Disadvantage of Designing for Minimum Noise Figure

As can be seen by Equation 4, there is only one load impedance, Z_L , that will provide a conjugate output match for a device terminated at the input for minimum noise. With the output terminated with a (conjugate) matched Z_L , the input impedance Z_{in} can be calculated according to Equations 6 and 7.

$$\Gamma_{\text{in}} = S_{11} + S_{12} S_{21} \Gamma_L / (1 - S_{22} \Gamma_L) \quad (6)$$

$$Z_{\text{in}} = Z_0 (1 + \Gamma_{\text{in}}) / (1 - \Gamma_{\text{in}}) \quad (7)$$

LNA INPUT MATCH

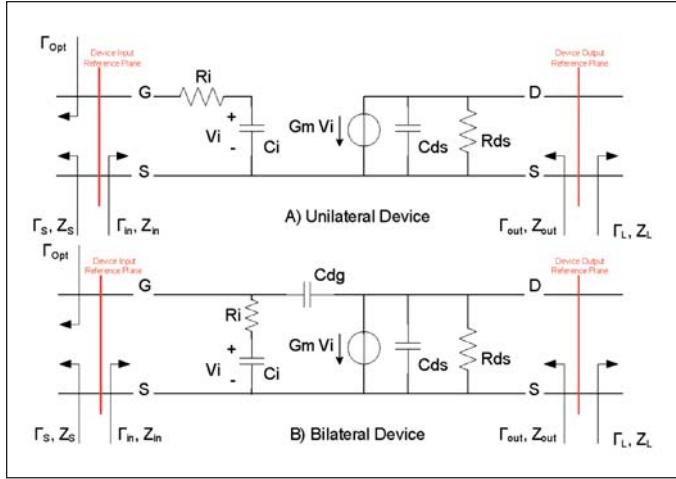


Figure 3 . Simple device model.

However, Z_{in} generally is not equal to Z_{opt}^* and so a mismatch occurs at the input port. Therefore, the disadvantage of designing an LNA for minimum noise figure (and maximum associated gain) is that the input will usually be mismatched.

The amount of mismatch, M, and reflection coefficient, Γ , can be calculated from Equations 8 and 9 respectively [4]:

$$M = (1 - |\Gamma_{in}|^2)(1 - |\Gamma_S|^2)/|1 - \Gamma_{in} \Gamma_S|^2 \quad (8)$$

$$\Gamma = \sqrt{1 - m} \quad (9)$$

The mismatch expressed in terms of return loss is:

$$RL = 20 \log(|\Gamma|) \quad (10)$$

For minimum noise, $\Gamma_S = \Gamma_{opt}$, and the return loss for this mismatch is (eq. 11):

$$RL = 10 \log[|1 - (1 - |\Gamma_{in}|^2)(1 - |\Gamma_{opt}|^2)/|1 - \Gamma_{in} \Gamma_{opt}|^2|] \quad (11)$$

Input Mismatch in the Unilateral Low Noise Amplifier

For the simplified unilateral device model shown in Figure 3A, $Z_{in} = R_i - jX_{Ci}$. The required input match for gain and best return loss would be $Z_S = Z_{in}^* = R_i + jX_{Ci}$. As stated previously, the required match for minimum noise is $Z_S = Z_{opt}$. Since there is no control over Z_{opt} or Z_{in} for the unilateral device, there is no way to achieve the noise and gain/RL match simultaneously. The resulting mismatch occurs with RL according to Equation 11. Without feedback the unilateral device will not allow for improving the input match without compromising the noise figure. Therefore, the method described next will not work for a unilateral device where $S_{12} = 0$. However, for most trans-

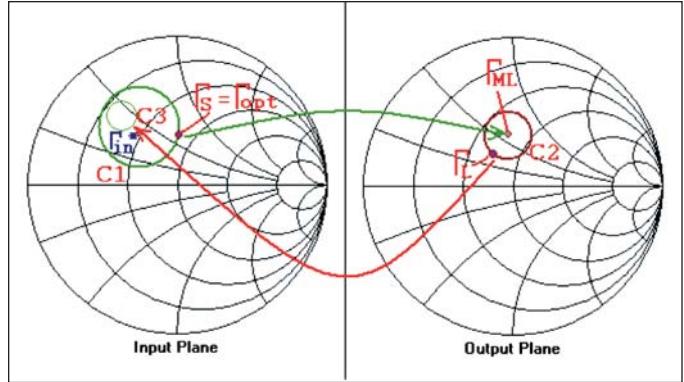


Figure 4 . Circle and impedance mapping on the Smith chart.

sistors $S_{12} \neq 0$ and the method in Figure 3 applies.

Trading Output Match for Improved Input Match

Consider the addition of C_{dg} (or other feedback mechanism) in the bilateral device model of Figure 3B. This feedback allows changes at the device output to be coupled to the input, thus changing the value of Z_{in} . If we can change Z_{in} to make it closer to Z_{opt}^* then we have improved the input return loss (while maintaining the minimum noise figure).

The exact dependence of $Z_{in} (\Gamma_{in})$ on $Z_L (\Gamma_L)$ was given in Equations 6 and 7. From this relation and the picture of the bilateral device model in Figure 3B, it is clear that some change in Z_L (the load match) will result in Z_{in} moving closer to Z_{opt}^* . The main question now is what values of load impedance (Z_L) will result in improved values of Z_{in} .

One value of Γ_L (if it exists) is certain to make $Z_{in} = Z_{opt}^*$. It can be found by solving Equation 6 for Γ_L in terms of Γ_{in} and the device S-parameters as shown in Equation 12:

$$\Gamma_L = (\Gamma_{in} - S_{11})/(S_{12} S_{21} - S_{11} S_{22} + S_{22} \Gamma_{in}) \quad (12)$$

Substituting Γ_{opt}^* for Γ_{in} in Equation 12 produces the correct load (Γ_L) for a perfect input RL match and noise match. There are a couple of problems with this approach. It can produce a very poor output match, often with a RL of only a few dB or even worse. Another potential problem is that the required load may not exist within the Smith chart boundary and therefore will not be realizable.

What is desired is a method that implements a compromise between perfect output return loss and poor input return loss and vice versa. Referring to Figure 4, the graphical solution is as follows:

1. Plot Γ_{opt} on the input plane (Smith chart representing impedances at the device input).

2. Map Γ_{opt} from the input plane to what would be a conjugate match (Γ_{ML}) on the output plane using Equation 4.
3. Plot a mismatch circle (C2 in Figure 4) relative to Γ_{ML} in the output plane. Any size circle can be used initially, but a circle representing a 1.5 VSWR makes a good starting point.
4. Map the output mismatch circle to the corresponding Γ_{in}^* circle (C3 in Figure 4) using the conjugate of Equation 6.
5. Find a point on C2 that maps to a point on C3 that is closest to $\Gamma_S = \Gamma_{\text{opt}}$. Denote the point on C3 as Γ_{in}^* .
6. Construct a mismatch circle (C1 in Figure 4) relative to Γ_{in}^* (found in step 5) that intercepts the point $\Gamma_S = \Gamma_{\text{opt}}$ in the input plane.
7. Compute the equivalent input return loss represented by circle C1 according to Equations 8, 9, and 10. Compute the equivalent output return loss represented by circle C2 in the output plane using similar expressions (in terms of Γ_{ML} and Γ_L).
8. Determine if the input and output return loss results of step 7 meet performance requirements. If not, repeat steps 3 through 8 using a different output mismatch circle C2. If the return loss at both ports is acceptable then proceed to design the

matching networks to yield $\Gamma_S = \Gamma_{\text{opt}}$ at the input and Γ_L at the output.

After designing the matching networks and bias feeds, the LNA design is complete. A simulation can be run on the complete LNA circuit to verify performance. All of the above steps (1 through 8) are automated in the LINC2 LNA Circles Utility. Selecting “Minimum Noise|F_{min}, Gain and RL” from the view menu performs all these steps in less than one second. A slider control makes the process interactive and intuitive. Moving the slider control from Max Output RL toward Max Input RL makes the tradeoff between output and input return loss automatic. The new match points, all circles, gain, return loss and noise figure are instantly updated when the slider control is moved.

The LINC2 Circles Utility allows for inputting an exact numerical value for the output return loss instead of using the slider control. Simply press the Enter key, input the desired output return loss, and click OK. Once again, the new match points, all circles, gain, return loss and noise figure are instantly updated. When the desired tradeoffs have been made, selecting the Match menu automatically designs the matching networks and synthesizes the complete LNA circuit schematic.

High Frequency Design

LNA INPUT MATCH

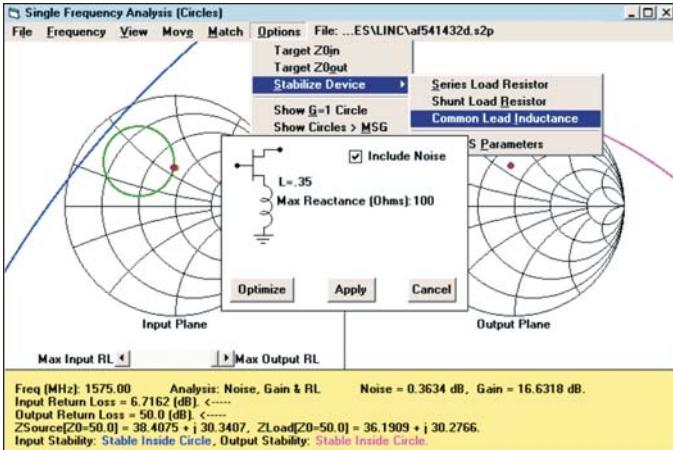


Figure 5 . The LINC2 LNA Circles Utility inductive feedback selection.

Balancing LNA Performance Among Noise Figure, Input Match and Output Match—A Three-Way Tradeoff

In the last section, a procedure was outlined for trading output RL for improved input RL while maintaining the NF at F_{\min} (minimum noise figure). That procedure is slightly restrictive since the input match impedance (Z_S) is not allowed to deviate from Z_{opt} . If the two-way tradeoff of the previous section is expanded to a three-way tradeoff between NF and RL at both ports, the added flexibility in allowing Z_S to vary away from Z_{opt} increases the capability of meeting more demanding RL goals at both ports.

It is often the case that giving up just a little in noise figure can go a long way toward boosting the input return loss without having to sacrifice too much output return loss. This is especially true when the noise resistance of the device is small. This is evident by noting in Equation 3 that the normalized noise resistance (r_n) is a direct factor in how the magnitude of the difference in Γ_S and Γ_{opt} adds to F_{\min} . When r_n is small, a small departure from F_{\min} results in a relatively large noise circle. For a given NF, this allows Γ_S (on the given NF circle) to reach closer to the point of best input return loss. In any case, giving up some NF improves the output to input RL tradeoff regardless of the value of r_n .

LNA Design Example

In addition to implementing the two-way tradeoff between input and output RL, the LINC2 program also automates the three-way tradeoff between NF, input RL and output RL. The procedure is similar to the 8-step procedure outlined above, except that a noise circle representing a noise figure larger than F_{\min} will be added. In this case, Γ_S will then be located on the noise circle at a point closest to the maximum input RL point,

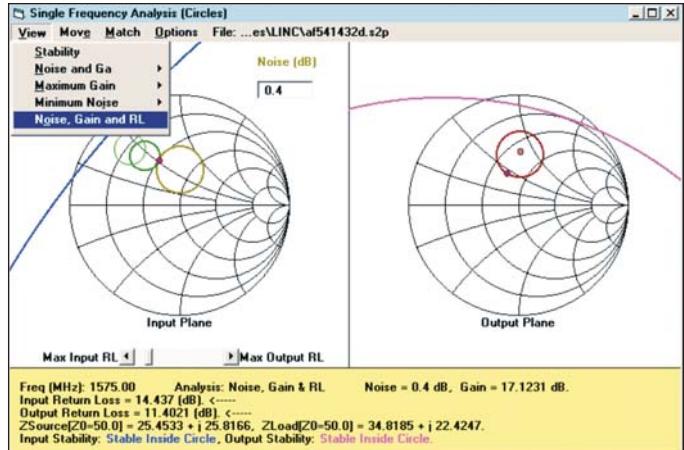


Figure 6 . Gain, noise figure and return loss tradeoffs using the Circles Utility.

instead of Γ_{opt} .

The proposed LNA design example will have the following design goals:

LNA Device: Agilent ATF-54143 FET PHEMT.
 DC Operating Point: $V_{ds} = 2$ V, $I_d = 20$ mA
 GPS Frequency Band: 1574.42 to 1576.42 MHz
 Power Gain: >16 dB
 Noise Figure: <1.0 dB
 Input RL: >13.98 dB (1.5 VSWR)
 Output RL: >9.54 dB (2.0 VSWR)

The design procedure will be implemented at 1.575 GHz (center of the GPS RX band).

The design starts by selecting “Amplifier Design | Low Noise Amplifier” from the LINC2 Tools menu. At the prompt the S-parameter file name for the ATF-54143 FET device is entered and the LINC2 Circles Utility opens with the device data loaded (Figure 5). The next step is to enter the frequency range (1574–1576 MHz) and select 1575 MHz from the Frequency menu as the design center frequency.

“View | Stability” displays stability circles for the selected frequencies, indicating that the design could benefit from increased stability. The LINC2 LNA design utility offers several methods for automatically stabilizing a device. When a stabilization method is selected from the “Options | Stabilize Device” menu, clicking “Optimize” will generate just enough resistive loading or inductive feedback to stabilize the device. For this example, 0.35 nH of common lead inductance was used for improved stability via series feedback. The 0.35 nH inductor is placed between the source (common) lead and ground as shown in Figure 5. In this example the inductance value was selected manually (instead of using Optimize) in order to control the amount of feedback short of complete uncon-

LNA INPUT MATCH

Specification	Goal	Design
Frequency	1575 MHz	1575 MHz
Power Gain	>16 dB	17.12 dB
Noise Figure	<1.0 dB	0.4 dB
Input RL	>13.98 dB	14.4 dB
Output RL	>9.54 dB	11.4 dB

Table 1 . Performance goals and results for the design example.

ditional stability.

Selecting “View|Noise, Gain and RL” from the top menu bar opens the Single Frequency Analysis (Circles) window for automated three-way tradeoff analysis between noise figure, gain and return loss (Figure 6). The printed data at the bottom of the window in Figure 5 indicates that the minimum noise figure at this frequency is 0.36 dB with a maximum associated gain of 16.6 dB. With the output matched (output RL = 50 dB), the input RL is reported as only 6.7 dB.

At this point only two things need to be done to meet the original LNA design goals. First, we trade off a very slight amount of noise figure for improved matching conditions. This is done by entering 0.4 dB in the Noise (dB) input box in the upper right corner of the Input Plane display (Figure 6). Then, the RL slider control is moved from Max Output RL toward Max Input RL until the input RL spec of 14 dB is exceeded. As the RL slider control is moved, the output mismatch circle grows while the input mismatch circle decreases in size. A check of the output RL indicates that it also exceeds the 9.54 dB spec by nearly 2 dB.

As the Noise, Gain and RL analysis of Figure 6 indicates, all specifications have now been met or exceeded as shown in Table 1.

The LINC2 program graphically and numerically displays the source and load impedances required to realize the design goals listed in Table 1. Z_S is plotted as a point at the intersection of the 0.4 dB NF circle and 14.4 dB RL circle. The exact source impedance is printed at the bottom of the window as $Z_{Source} = 25.45 + j25.82$ ohms. Z_L is plotted as a point on the 11.4 dB output RL circle. The exact load impedance is printed at the bottom of the window as $Z_{Load} = 34.82 + j22.42$ ohms.

The displayed Z_S and Z_L data is required information for designing the input and output matching networks. However, LINC2 automatically takes this data and synthesizes the complete LNA schematic including the matching networks and device stabilization components.

LINC2 LNA Synthesis

The LINC2 LNA design module offers many approaches to low noise amplifier design and synthesis. The fol-

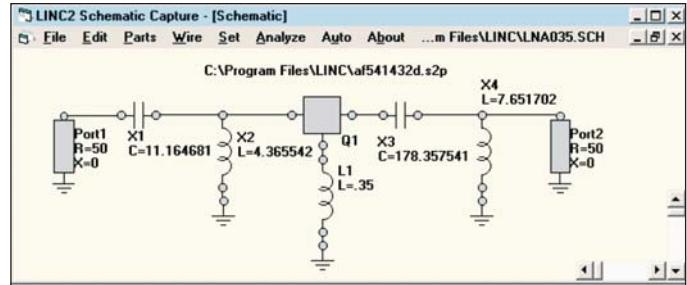


Figure 7 . LINC2 synthesized LNA schematic.

lowing design methods are automated in the LINC2 LNA design tool:

- Minimum noise
- Maximum gain
- Noise and gain tradeoffs (match varies between F_{min} and Γ_{max} points)
- Minimum noise with improved input RL (trading off output RL)
- Low noise with improved input RL (trading off NF and output RL)
- Available power gain design
- Operating power gain or transducer power gain design

As is the case for each of these design methods, the three-way design tradeoff presented above is completed by simply selecting the desired matching network topology from the Match menu. An LNA schematic is immediately synthesized that captures the design’s performance. When a lumped L network with a series C and parallel L topology is selected from the Match menu, the LNA schematic in Figure 7 is generated.

Clicking Analyze in the schematic window runs a circuit simulation producing the results shown in Figures 8

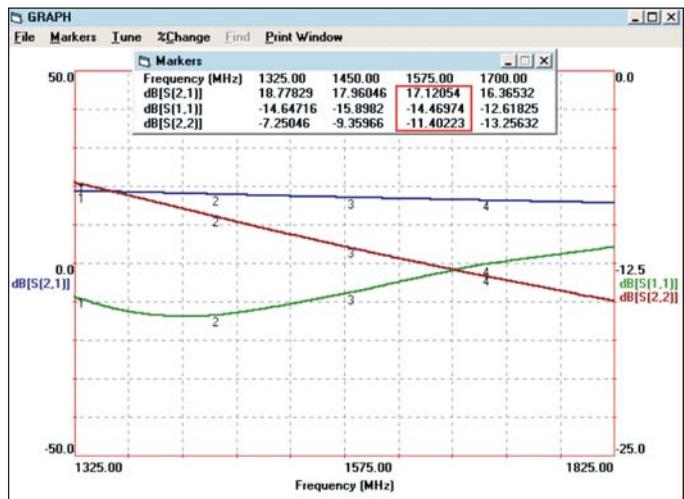


Figure 8 . Gain (S_{21}) and return loss simulation results.

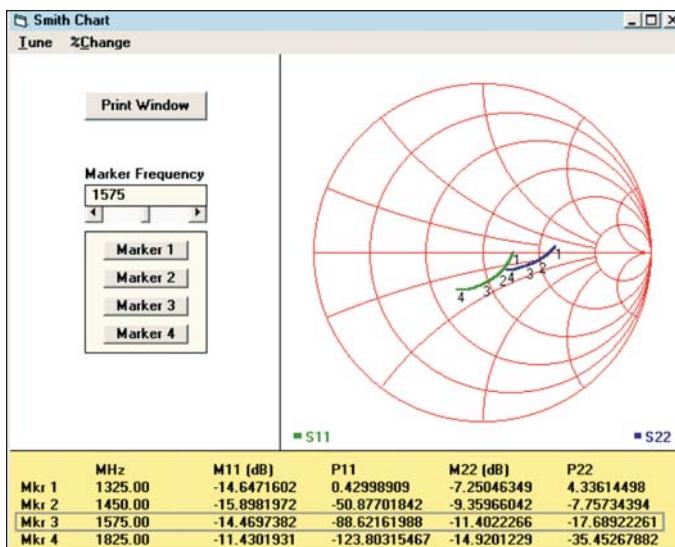


Figure 9 · Input and output return loss simulation results.

and 9. The simulation results for the design frequency of 1575 MHz were exactly as predicted with gain = 17.12 dB, input RL = 14.4 dB and output RL = 11.4 dB.

The next step is to add the bias networks and construct the 0.35 nH source lead inductor from microstrip transmission lines and ground vias as shown in Figure 10. The component values in Figure 10 have been changed to the nearest available standard value. The shunt input inductor is connected to the gate supply and a 68 nH choke is used to supply DC to the drain.

Design Verification

Running a simulation of the LNA circuit in Figure 7 provides a certain level of design verification since the computer methods and algorithms used in the LINC2 circuit simulation are very different and independent from the synthesis algorithms used to generate the design in Figure 6. Ultimately, however, the design must be verified by building a prototype and testing it. The circuit in Figure 10 was built and tested. The measured performance was remarkably close to the results obtained from the LINC2 circuit simulation (Table 1, Figures 8 and 9).

The measured versus simulated results are shown in Table 2. Figure 11 plots the simulated and measured gain

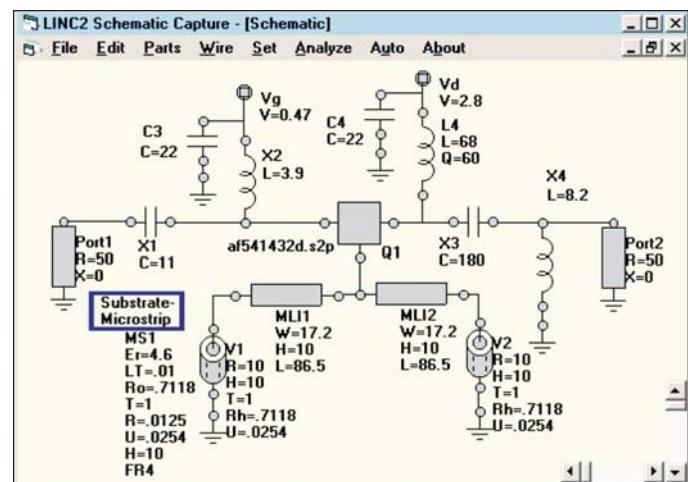


Figure 10 · Prototype LNA circuit schematic.

and noise figure. Figure 12 plots the simulated and measured input and output return loss. The measured gain, NF and input RL agreed with simulation within a fraction of a dB. The output return loss measured lower than the simulated value by about 1.25 dB.

Summary

This LNA design example demonstrated how the unique features of the LINC2 LNA design tool can simplify the complex task of balancing a number of competing design tradeoffs. LINC2's automated interactive optimization at the design level (during the circuit synthesis procedure) can be far more effective than circuit level optimization. In addition to being faster than circuit level optimization, interactive optimization at the design synthesis level allows for optimization of the circuit topology, not just the component values of a given topology. For example, circuit level optimization starts with a given circuit topology while in the LINC2 LNA synthesis tool the circuit topology (matching networks) are selected last, after all tradeoffs have been made and the design has been optimized.

It is not uncommon for leading RF/microwave EDA software packages to have utilities for plotting various circles on a Smith chart to aid in the design of low noise amplifiers. However, these other circle plotting tools are

Specification	Goal	Simulation				Measured		
		1574	1575	1576	1574	1575	1576	1576
Frequency (MHz)	1574 - 1576	1574	1575	1576	1574	1575	1576	1576
Power Gain (dB)	>16	17.13	17.12	17.11	17.75	17.74	17.71	17.71
Noise Figure (dB)	<1.0	0.4	0.4	0.4	0.68/0.38*	0.67/0.37*	0.66/0.36*	0.66/0.36*
Input RL (dB)	>13.98	14.48	14.47	14.46	14.03	14.02	14.02	14.02
Output RL (dB)	>9.54	11.39	11.4	11.42	10.18	10.17	10.17	10.17

Table 2 · LNA simulated versus measured results. *NF after adjusting for 0.3 dB total front-end component losses in cable, connector and input microstrip.

LNA INPUT MATCH

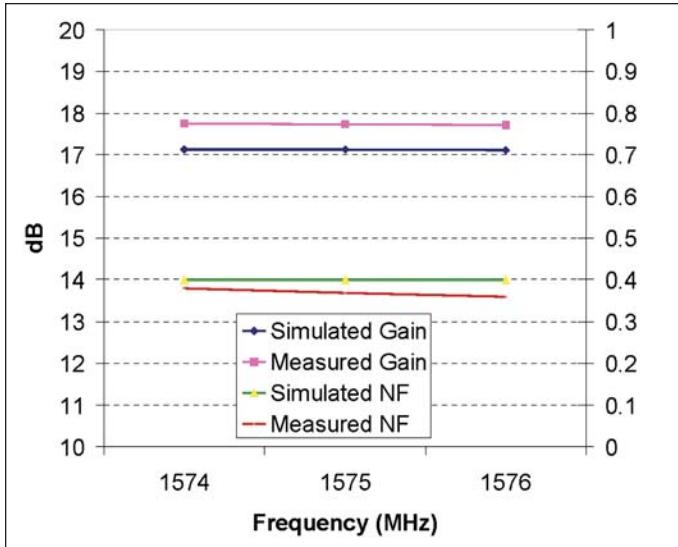


Figure 11 . LNA simulated and measured gain and noise figure.

usually manual in nature in the sense that they require the user to know what circles to plot and how to relate the circles to one another and to the design flow. The LINC2 Circles Utility is completely automated and linked to the design flow. This allows the user to focus on the design goals and the parameters that affect performance rather than on the construction of circles.

The underlying math routines and LINC2 proprietary algorithms keep the circles and printed design and performance data updated as the user enters specifications or makes design tradeoffs. This highly automated LINC2 design tool makes the various constant circles practically obsolete because the user is guided through the design procedure without having to construct the circles or even having to know what they mean. However, experienced designers who are accustomed to designing LNAs by manipulation of the constant circles will appreciate the visual feedback provided by the automatically displayed circles and the fact that they can also be manually constructed by the user if desired. This kind of graphical feedback can help the user know what is possible in regard to performance and why. This level of insight into the parameters that affect the design and its performance as well as the insight into the design methods and synthesis process cannot be provided by simply using a circuit level optimizer.

LINC2 is a high performance, low cost, RF and microwave design environment providing automated

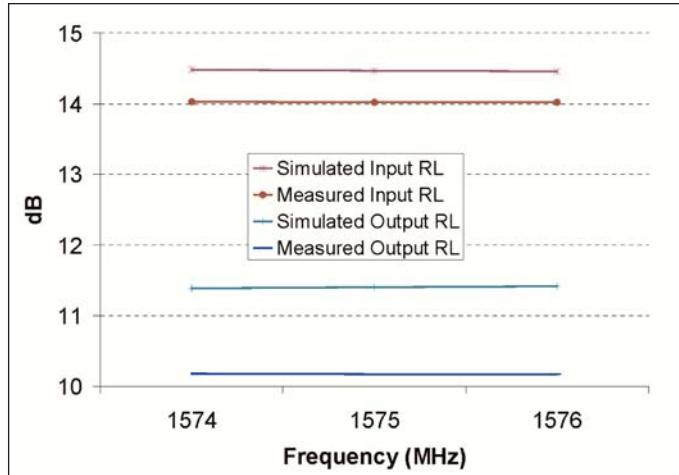


Figure 12 . LNA simulated and measured return loss.

design, circuit synthesis, schematic capture, simulation, optimization and yield analysis in one integrated package. LINC2 is available from Applied Computational Sciences at: www.appliedmicrowave.com.

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