

Things to Consider in the Transition to Chip-Level Design

By Gary Breed
Editorial Director

Designing on GaAs, SiGe, CMOS or plain old silicon requires an awareness of the limitations (and possibilities) presented by small, semiconductor substrates. An inquisitive, problem-solving mindset helps, too!

Is your company making the change from p.c. board and alumina substrates to integrated circuits (RFIC/MMIC) and system-on-chip (SoC) technology? Are you upgrading your skills to add chip-level design to your proven circuit

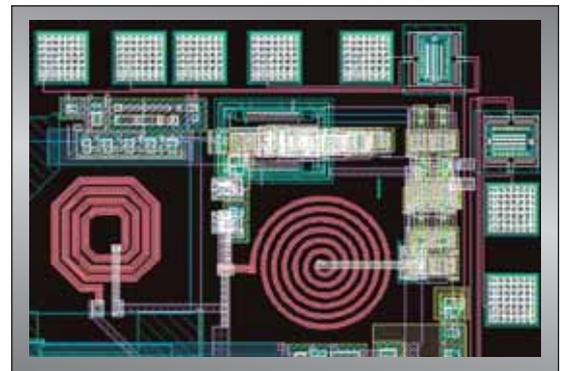
design abilities? If so, this tutorial is intended to begin that learning process. We can't teach you everything in two pages, but we can make you aware of some of the important things that are different when designing on a semiconductor substrate instead of classic RF and microwave circuits.

The single biggest area of difference is in passive components, which is where this discussion will start.

Size Matters

One of the reasons for designing an IC is to save space compared to a discrete or hybrid design. While this is good for reducing parasitics, it places limits on the physical size of passive components. The maximum obtainable values of on-chip capacitance and inductance may require you to use off-chip components, especially at lower frequencies where resonant circuits require much greater L and C values.

It may be possible to eliminate some or all of the off-chip components with different design architecture. For example, direct conversion eliminates filtering and matching components associated with an intermediate frequency. This RF simplification comes at the cost of greater complexity in the baseband



When your designs look like this instead of discrete components on a p.c. board, there are many different design techniques and constraints on available component values.

processing, where DC offset, phase shift corrections and channel filtering are applied. These, and other, design tradeoffs depend on system performance requirements as well as the cost, power consumption and footprint of the additional signal processing circuitry.

Some designers who have made the transition to chip-level design have become fascinated with the new problem-solving requirements. Before, they could select components and eventually create a near-perfect solution for their design criteria—as long as time, cost and size were low priorities. Now, each new task is a puzzle to be solved, which can be a satisfying challenge.

Finally, size is much less of a consideration when the wavelengths involved are suitable for sizes in the cm^2 range. In fact, part of the reason for development of the earliest MMICs was to take advantage of the scaling down to chip size for microwave and mm-wave circuits.

Yes, They're Really "Semi"-conductors

Another limitation is in the materials used for RFICs and MMICs. Designs at the chip level do not have the luxury of low-loss dielectrics with whatever dielectric constant is most suitable for the task. At best, you'll have an insulating oxide layer that is not as bad as the primary material. You might use MEMS-type processing that allows air bridges and suspended conductors, but it will cost a lot more. Semiconductor-on-insulator technologies are another possibility for improving on the low inductor Q and losses of standard semiconductor processes.

Mainly, a design engineer will be forced to deal with the limitations presented by standard semiconductor material and process. These alternative processes are typically reserved for applications where performance is paramount.

Another important matter is simple resistors. A silicon resistor is OK, but often it's actually easier to fabricate transistors than resistors. A specific result is that ICs often employ active bias circuits instead of the resistor networks that would be used on a p.c. board without even stopping to think about it. Examine some of the equivalent circuits of standard building-block RFICs and you will see transistors used in places where you would think

two simple resistors would get the job done. With transistors, your design approach should always be to think first in terms of current, before considering voltage.

Another change in mindset is adjusting to having as many transistors as you want. Discrete designs usually minimize the semiconductor component count for reasons of cost, complexity and reliability. (The transistors are always the first things to blow up, right?) On an IC, especially on the silicon processes, general-purpose transistors are trivial, so go ahead and use them for biasing, feedback, switching, impedance shifting and isolating.

Engineering at the Molecular Level

It's been said that integrated circuits are made by physicists, not engineers. Of course, that's only true of the fabrication part of the job—functional design is definitely an engineer's primary task. However, any engineer designing at the chip level is advised to learn as much as possible about the physics of the family of "components" he or she will be using.

It is certainly possible to get by using the foundry's specs for individual transistors, metallization, capacitors, resistors and other devices. Their simulation and design verification toolkits contain the accumulated physical knowledge necessary to confirm that your design will work. But understanding foundation principles always makes it easier to apply the specs wisely. Such factors as current density, junction temperature, and process variations may prompt you to make adjustments to the design to avoid subtle effects—not an essential job, but one that can make a difference in yield and long-term reliability.

Apply EM Simulation and Analysis

This is the final topic because it's the final step in your design. The condensed size of an integrated circuit increases the coupling between adjacent circuit elements. Electromagnetic simulation will identify signal currents, coupling and radiation, both desired and undesired. You will almost certainly be doing this for those portions of the circuit that employ microstrip or stripline structures, filters, couplers and inductors. Continuing that analysis to the rest of the circuit will increase confidence that it will function as desired with (hopefully) no need for design modifications.

All RF/microwave/high-speed digital semiconductor processes are extensively supported by EDA tools. All these tools include, or can link to, several types of EM simulation engines. Just like a classic hybrid circuit, you'll need to decide when to use the speed of planar analysis, the accuracy of full-wave 3D simulation, or the time-domain insight of FDTD analysis.

And when the design is finished, enjoy the results contained in that tiny package the same way you did with a big p.c. board or ceramic hybrid.