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Active Multiplier Realization Using Harmonic Loading at Ku-Band

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This article describes a frequency tripler that replaces the typical idler circuit with a recently-developed filter structure

Signal generation is one of the most critical problems in the microwave and millimeter-wave communication market. The demands of greater stability and low phase noise further increase complexity in the circuit design. Signal generation in the millimeter-wave bands can be realized either directly by an oscillator or by multiplication from a lower frequency. An effective solution is to multiply the output of a low noise oscillator. FET frequency multipliers appear attractive compared to diode multipliers because of their potential to have better conversion loss and output power, along with their compatibility with MMIC processes [1]. Moreover, HEMT is the preferable choice in the family of the transistors due to its higher cut-off frequency, better noise characteristics and mature technology both as a discrete device and in MMIC configuration.

Mostly, active multipliers have been configured as frequency doublers, although many system configurations operating in the millimeter-wave ranges may require frequency triplers. Still, developing frequency triplers with low drive, low loss and simplicity in design is still a challenge at the higher end of microwave frequencies. The high RF input power might effect the lifetime of the transistor due to rectified current in the gate-channel junction. Also very little has been discussed concerning the agreement between simulated and practical results, particularly for bias operation. This article discusses the approach in designing a frequency tripler using a HEMT device at Ku band, in MIC configuration, keeping simplicity and repeatability as prime considerations by incorporating a harmonic loaded band pass filter at the output.

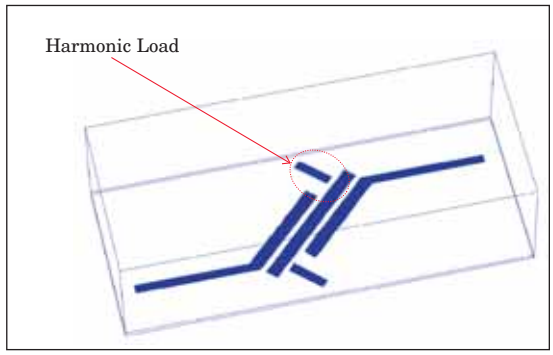

Figure 1 · Structure of the harmonic loaded bandpass filter.

Harmonic Generation in FET Triplers

Two fundamental approaches to generate frequency multiplication are commonly employed, i.e., choice of appropriate biasing and proper conduction angle for getting the desired multiplication order [2, 3]. Any class of operation with proper biasing can give the desired harmonic order but the choice depends upon some critical parameters like ease of operation, circuit simplicity, repeatability and I-V excursion within device acceptable ratings. Class-C operation with the optimum conduction angle of 80º maximizes the third harmonic content but this mode of operation requires high breakdown voltage. Class-B operation has also been explored but either it increases circuit complexity by using fundamental rejection feedback topology at the output or uses high input drive to get the desired output power [4].

Class-A operation based on the distorted drain voltage waveform provides higher odd harmonic current by providing short circuit at the even harmonics and open circuits for the odd harmonic except the desired third harmonics. This is the easier and efficient technique but the major constraint in this approach is placing quarter wavelength transformers for short-circuiting the even harmonics. This increases the circuit complexity as impedances at other harmonics also have to be taken into account and should be tuned out. This approach also needs extensive simulation using CAD tools. In this article the concept of harmonic loading of overloaded band pass filter has been implemented having minimum stub requirement.

Circuit Design and Analysis

A complete tripler design consists of implementation of the accurate model parameters in the CAD tool, output filter design and matching circuitry along with proper biasing and its position reflects in close match with the simulated values [5].

HEMT Non-Linear Model

Non-linear model is a critical part in any harmonic balance analysis. The present work in this paper assumed non linear characteristics of the HEMT model to be similar to a MESFET. The extrinsic part is related to device layout and modeled with linear elements. The intrinsic part is represented by non-linear currents and charge generated conduction and displacement currents. I-V curves for different transistors have been taken for proper DC characterization. AC parameters were found by overall measured performance (both small signal and large signal analysis) of the sampler circuits. A Materka model has been generated with the lumped sparse modeling tool of the CAD software Linmic, suited for the multiplier operation. The choice for choosing the Materka model lies in its better representation of the saturated output power. Some major parameters representing zero bias threshold, DC current saturation, peak transconductance, output conductance, reverse saturation and saturated input transcapacitance and output capacitance were fine tuned to get an accurate model detailed in Ref. [7] The inductance due to DC bias wire along with the inductance from the device leads has also to be modeled and incorporated in CAD tools for proper simulation.

Filter Aspects

The bandpass filter at $3f_0$ is separately designed, tested and incorporated at the output of the tripler. The filter is based on the overloaded topology to suppress the second harmonic. Using the harmonic loading concept in the overloaded filter [8, 9], the second harmonic is shorted out and capacitive loading is presented to the first harmonic, as determined using the electromagnetic simulator (LINMIC/SFPMIC) [10]. This provides the voltage distortion, which is high in odd harmonic current. This filter is incorporated at the output of the multiplier. Instead of a typical harmonic filter, the concept of harmonic loading eases circuit complexity while giving a clean spectrum. It has been optimized along with the phase shifter (adding simple line length to adjust the phase) to present a short cir-

The Harmonic Loaded Filter

For selection of harmonics in a multiplier circuit, the filter must pass the desired output signal frequency while suppressing unwanted harmonics of the fundamental. Microstrip filters are desirable for their compact, easy-to-build structures, but hairpin filters have inadequate harmonic rejection, and coupled-line filters may be larger than desired.

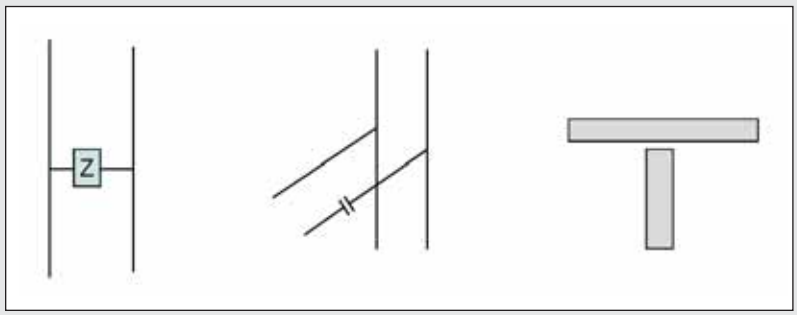

Figure A · Development of the stub filter used for changing filter response at a harmonic frequency with little effect in the passband.

The harmonic loaded filter uses stub resonators to augment the harmonic rejection. Figure A shows the development of the stub from a shunt impedance (left) to a capacitively-coupled stub (center), to its realization in microstrip with a gap providing the necessary capacitance (right). When combined with a coupled line filter, the resulting structure is that of Figure 1, also seen in the circuit of Figure 3. The stub has the effect of making a significantly more compact filter by eliminating the need for a separate idler circuit to suppress the second harmonic. The harmonic loaded filter has a response that is capacitive at the fundamental frequency, a short circuit at the second harmonic, while passing the desired third harmonic with only the normal filter loss. Of course, typical microstrip design considerations must be followed, including electromagnetic simulation.

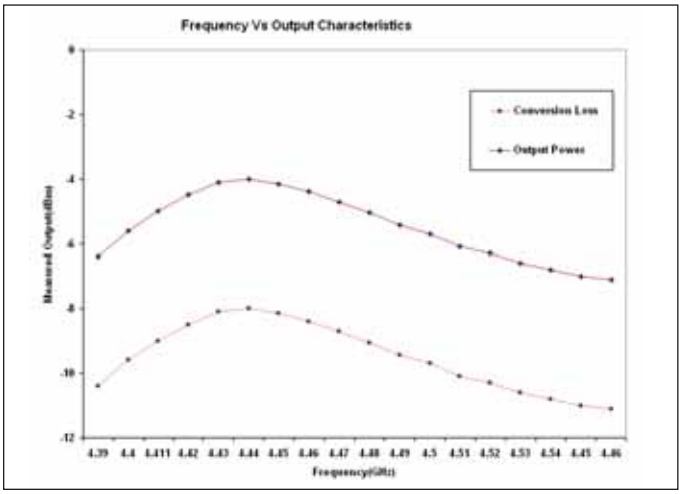

Figure 2 · Measured result of 13.5 GHz tripler.

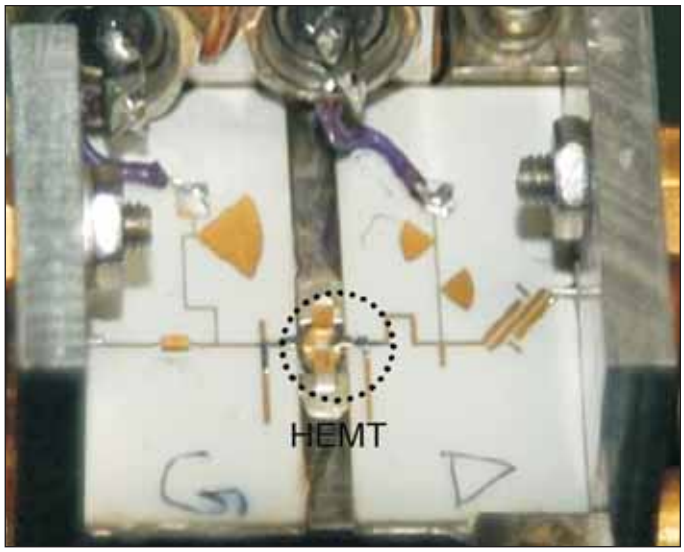

Figure 3 · Photograph of the tripler circuit. The harmonic loaded filter is visible on the right side.

cuit for the even harmonics and an open circuit at the odd harmonics except for the output harmonic.

Tripler Design

The tripler has been designed using the CFY-67-08 HEMT from Infineon, which is a low noise device. The input circuit is matched at the fundamental frequency f_0. Harmonic balance analysis incorporating a "dynamic load line" has been performed to have better understanding of the circuit performance. The major criterion for efficient tripler operation is the choice of bias, together with with the harmonic current feedback to the device. To get an asymmetrical output waveform rich in third harmonic energy, the approach adopted in this paper is biasing the device in class A and presenting short circuits at the even harmonics and open circuits at the odd harmonics, except for the third harmonic which is matched for maximum output power. The transmission line acting as a phase shifter in series with the bandpass filter provides a parallel resonance to the drain parasitics to maximize voltage at the harmonic frequency. The phase shifter, along with harmonic loaded topology of the filter, adjusts the impedance to higher values for fundamental, short-circuit for the second harmonic and transparent to the third harmonic, thus providing efficient multiplication.

Overall, the design is based on primarily three steps: non-linear device characterization, input match for the gain, and output match for harmonic selection and enhancement.

Measurement Results

The filter at the output frequency has been tested separately and then further optimized using electromagnetic tool (SFPMIC) of Linmic. The harmonic load is adjusted for suppression of even harmonics. The filter gives insertion loss of better than 1 dB with return loss better than 15 dB. The second harmonic ($2f_0$) is suppressed by more than 40 dB. The full circuit along with filter is etched on 10 mil alumina and attached to Kovar plate using conductive epoxy. The principal parameters of interests are the conversion loss, harmonic suppression and spectral purity. The harmonic balance technique of Linmic 6.3 [10] has been extensively used to simulate the entire circuit. The large signal analysis shows the trajectory at the output plane as an ellipsoid due to effect of a reactive load connected to the drain. At the extremes, the ellipsoid becomes distorted resulting in clipping of drain voltage and drain current. The input frequency is 4.5 GHz (f_0) and output is measured at 13.5 GHz ($3f_0$). The measurements were taken for different drain and gate biases. The class-A operation was used having V_{ds} = 1.5 V and I_{ds} = 12 mA. The measured results show the conversion loss of better than 10 dB in the 3 dB bandwidth of 200 MHz (Fig. 2). The input power typically required is +3 dBm for having good efficiency. The suppression at fundamental is better than 15 dB and second harmonic suppression is better than 25 dB. The output power comes out to be –5.5 dBm for an input drive of +3 dBm. This closely relates to the simulated values. The size of the circuit is 20 × 20 mm. A photograph of the completed tripler is shown in Figure 3.

Conclusion

This approach is validated by developing two active triplers at two different output frequencies 13.5 GHz and 17.1 GHz, respectively. The slight variation in frequency is found out due to fabrication inaccuracies. The generated model predicts the behavior of multiplier closely with the simulated results. Still, in the authors' knowledge, a

model predicting close match between simulated and measured results, with accurate bias prediction, has not been reported so far. In spite of the negative gain presented (due to device limitation), the losses are lower than obtained with an equivalent diode tripler, which may be around 20 dB. The results can be further improved by choosing different devices that have higher gain and cut off along with better breakdown characteristics. The present approach presents a circuit having optimum performance with a lower drive. This is achieved by using the harmonic loading concept in the filter. The concept can be easily extended to higher frequencies and MMIC fabrication.

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