LDMOS Power Modules for Two Way Mobile Radios

By Alfio Scuto

Providing both amateurs and professionals with the tools needed to create their own "two-way radio."

Abstract: Two-way radios are today present in almost every area of our public life. They are an invaluable tool supporting professionals in a wide range of industries ranging from transportation to energy, government and others. With two-way radios, there's no need to deploy supporting infrastructure in the field. In fact, two-way radios can offer an instant communication (private and cost-effective) anywhere and anytime. Nevertheless, there is a vast and growing market among non-professional users who demand high-quality yet affordable equipment. The purpose of this article is to provide both amateurs and professionals with the tools needed to create their own " two-way radio" not linked to any specific standard product present in the market. This allows greater integration in radio systems currently in development, and in general, a considerable saving on production costs.

Introduction

The article shows the design flow for two RF power amplifier modules working in the UHF band with the output power being the only main difference.

The name and target specifications of each project are the following:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VDD	Supply Voltage		12.5		V
F	Frequency Range	400	-	470	MHz
Pin	Input Power		5		dBm
η_T	Total Efficiency	50			%
2fo	2nd Harmonic			-45	dBc
ρ_{in}	Input Return Loss			-3	dB

Pout	Project's Name
45 W	STEVAL-TDR031V1
70 W	STEVAL-TDR034V1

Table 1 • Target specifications.

Both designs use Laterally Diffused MOS (LDMOS) devices respectively housed in three different packages: SOT-89, PowerFLAT, PSO-10.

In order to meet the above targets, a line-up topology with three power stages 2 has been used.

The basic idea was to consider the two projects as being a single project (Figure 1), where the cascade 1st and 2nd stage should have enough power to drive the final stage of the two devices in parallel.

Depending on the output power (see Fig: 1 project's name) the final stage has been designed with two devices in parallel, respectively: 2xPD85035S-E or 2xPD85050S.

Based on the two devices' datasheets (PD85035S-E and PD85050) we calculated that a 36 dBm power level is required to achieve a 45W or 70W output power.

Similarly, for the drive stage (cascade 1st and 2nd stage), using the datasheets for PD84002 and PD85006L-E, we obtained the following power level chain.

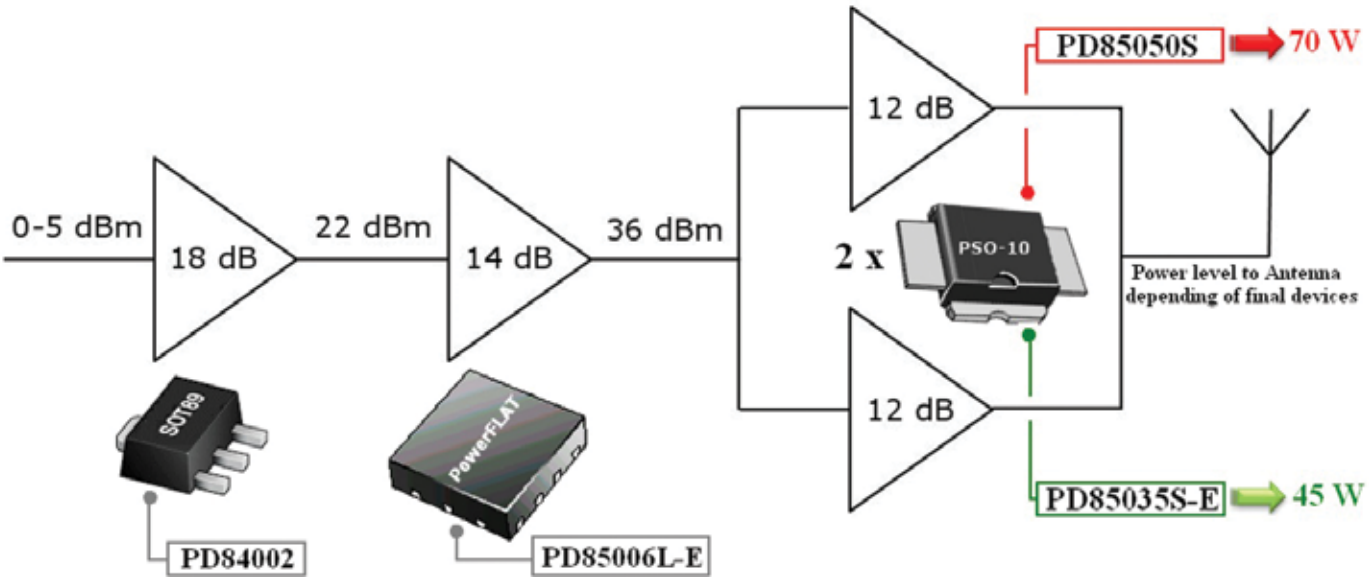

Figure 1 • Power level chain.

Each stage was simulated using the ADS software from Agilent. The intent was to get the right output impedance level to guarantee the desired power level all along the line-up.

Using library models available for each product employed (www.st.com/rf), several simulations were performed cascading the 1st and the 2nd stage in order to get a power level greater than 36dBm.

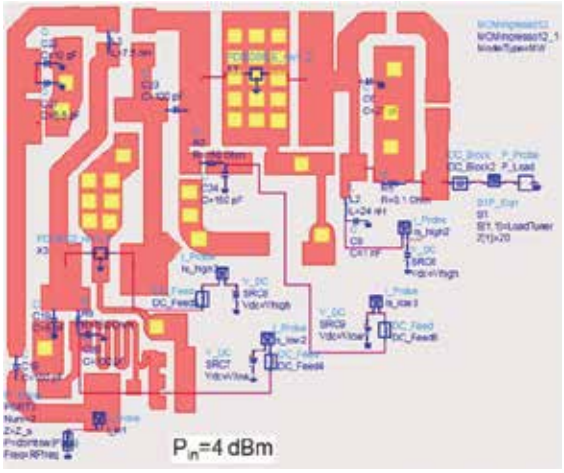

Figure 2 • 1st and 2nd stage.

Following the simulations at central frequency (435 MHz), the optimum load impedance for the final stage (2nd stage) is:

$$\begin{cases} Z_{source} = 50\ \Omega \\ Z_{lopt} = (3.818 - j * 1.189)\ \Omega \\ P_{delmax} = 38\ dBm\ (\approx 6.3\ W) \end{cases}$$

Using this impedance value at 435MHz (Zlopt) performance was optimized along the required frequency band. In Figure 4 we can observe that the level of the output power is higher than required. Later the level might drop due the effects of mismatching losses and/or losses in the stabilization network between the 2nd and 3rd stage.

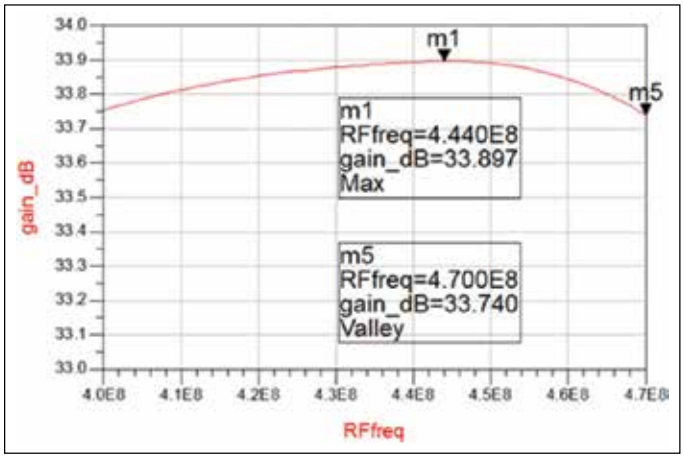

Figure 3 • Gain vs Frequency.

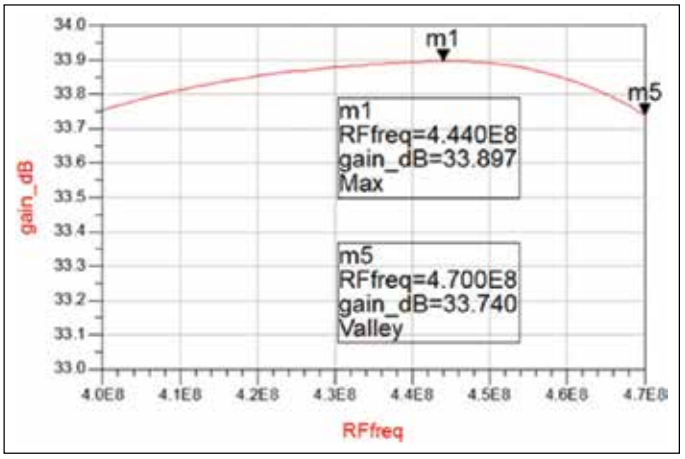

Figure 4 • Power vs Frequency.

Designing the Final Stage: Preliminary Trials Using Chip On Board

The two target projects (Table 1) were done using packaged LDMOS. Nevertheless it has been valuable to explore all the potential capabilities offered by the technology directly using the dice (no package). In this section we will analyze a hybrid combination between chip-on-board (COB) as final stage and two packaged products for 1st and 2nd stages.

Thanks to the COB solution analysis we have a better understanding of all the thermal aspects which are essential for this power stage.

To realize the module we have used the FR-4 substrate as dielectric (20 mils) bonded with a Copper metal plate (1.6mm) which ensures a very stable thermal condition for the power amplifier.

Figure 5 • Substrate.

On the top of the substrate FR-4 (dielectric) there are two openings where the two dice have been directly bonded on copper metal gold finished layer.

The wire bond diagram and dimensions (Figure 6) are similar to those used for the PD85035-E.

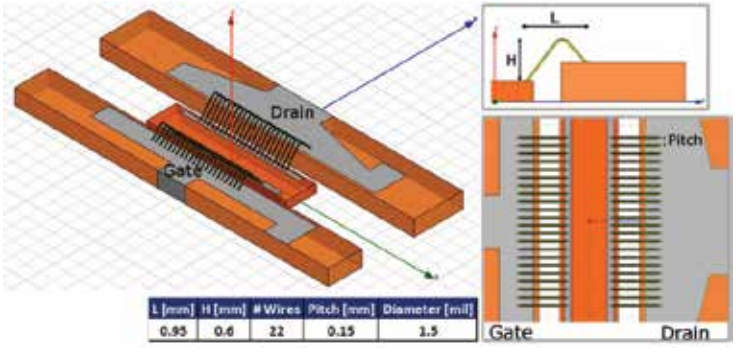

Figure 6 • Wire bond diagram.

The structure, dice and wire-bonding (Figure 6) has been simulated with HFSS to extract the equivalent lumped inductors on the gate and drain sides (Figure 7 and Figure 8).

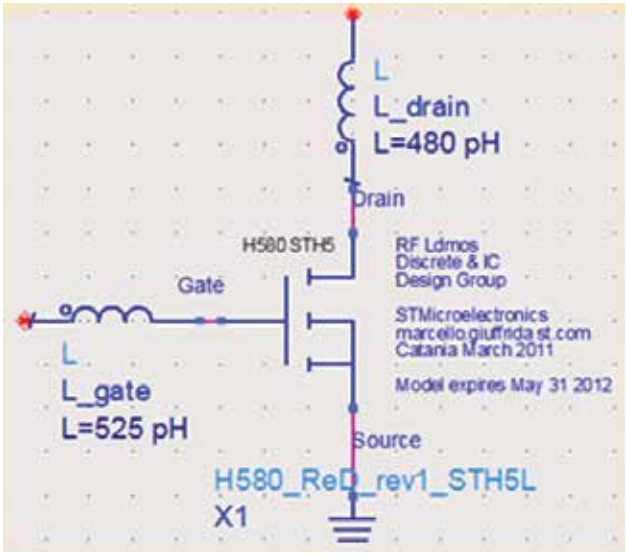

Figure 7 • Equivalent lumped inductors.

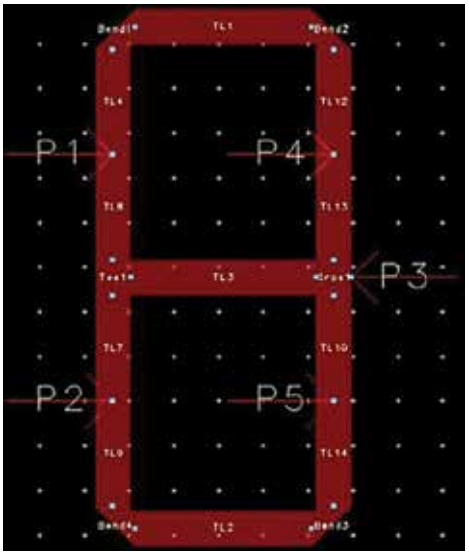

Figure 8 • CIT.

Another important aspect concerned the power combination of the two dice in parallel.

We had to look for a structure to accomplish a dual intent: increase the impedance level (impedance matching) and, at the same time, reduce the inevitable losses (power combination)

The idea was to combine the dice with the microstrip topology depicted in Figure 9. We will refer to this structure as Combiner and Impedance Transformer (CIT). Through simulation (Momentum) the physical dimensions have been optimized in order to get a symmetric structure and a good impedance transformation.

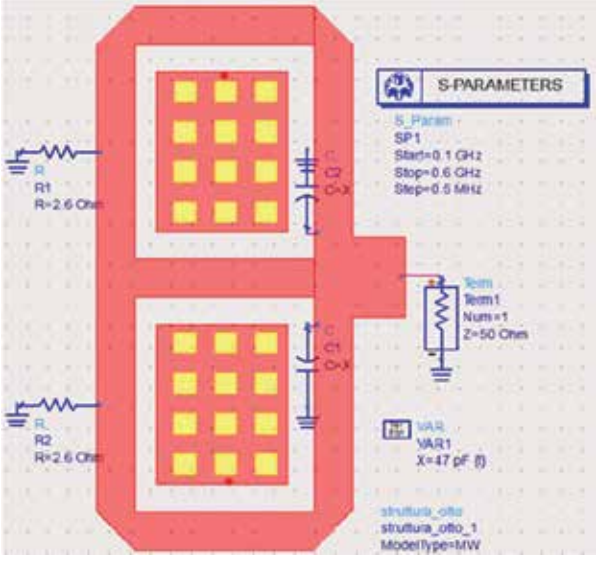

Figure 9 • CIT transformer.

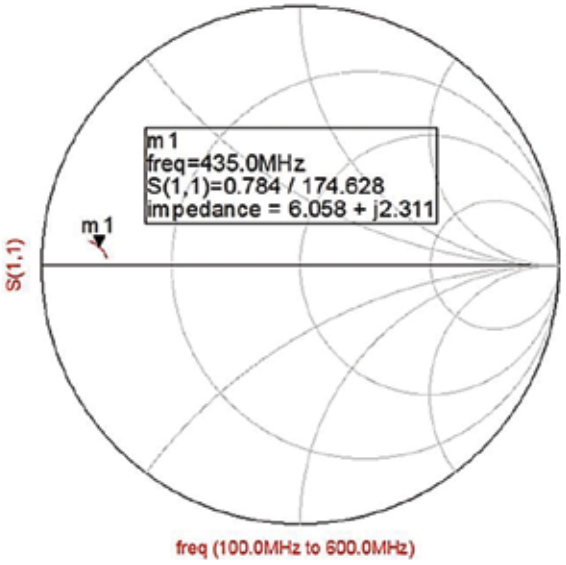

Figure 10 • Impedance Transformation of CIT.

To prove the benefits of the CIT as impedance transformer, it was employed in a simulation using as starting point the impedance at drain level of two LDMOS devices in parallel.

Using the Cripps' method 1 (load-line analysis) the impedance transformation of the structure was tested. For a single device, the power capability is:

$$P = \frac{V_{dc}^2}{2R_L} \rightarrow R_L = \frac{V_{dc}^2}{2P} = \frac{(13.6)^2}{2 \cdot 35} = 2.6\,\Omega$$

For two LDMOS devices in parallel the value must be divided by two.

The Smith chart confirms the good impedance transformation obtained (Figure 10).

At this point the CIT has been considered part of the active devices and simulated at 435 MHz with the load-pull (Figure 11).

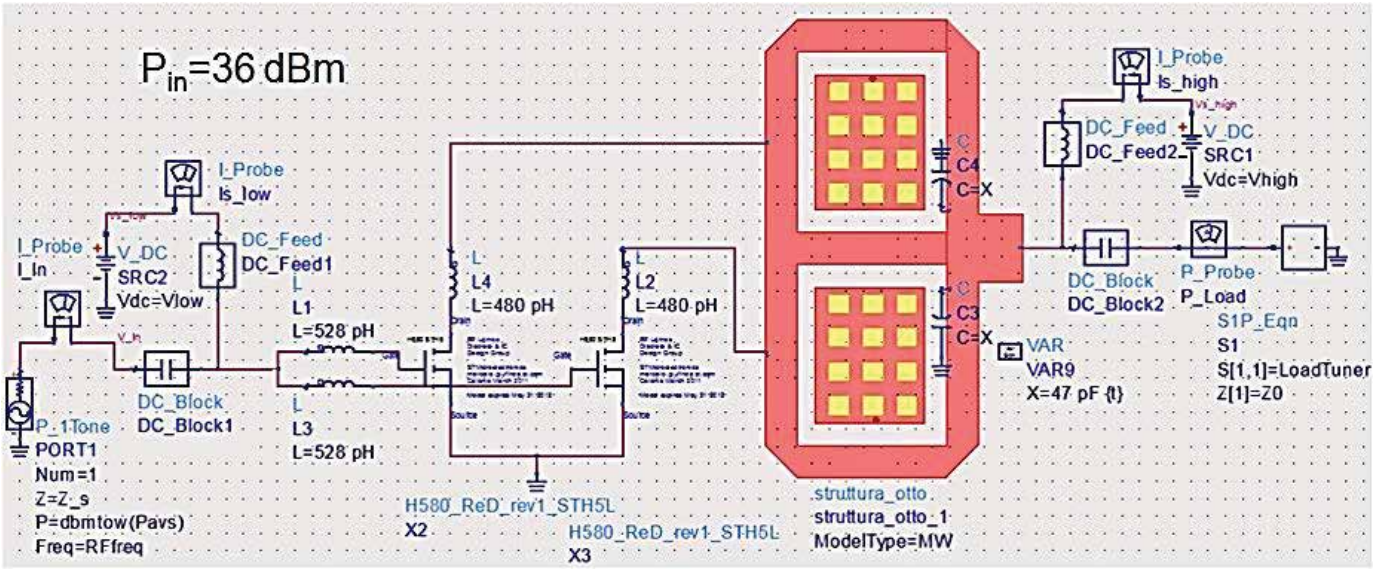

Figure 11 • Final stage simulation.

In the equation below ZLopt is the impedance to obtain Pdelmax.

$$\begin{cases} Z_{source} = 50\,\Omega \\ Z_{lopt} = (3.818 - j * 1.189)\,\Omega \\ P_{delmax} = 38\,dBm\ (\approx 6.3\,W) \end{cases}$$

Using the ZLopt just found, we did an optimization work to equalize the gain in band (Figure 12) and a power sweep at central frequency (Figure 13) in order to achieve more than 60 W at P3dB.

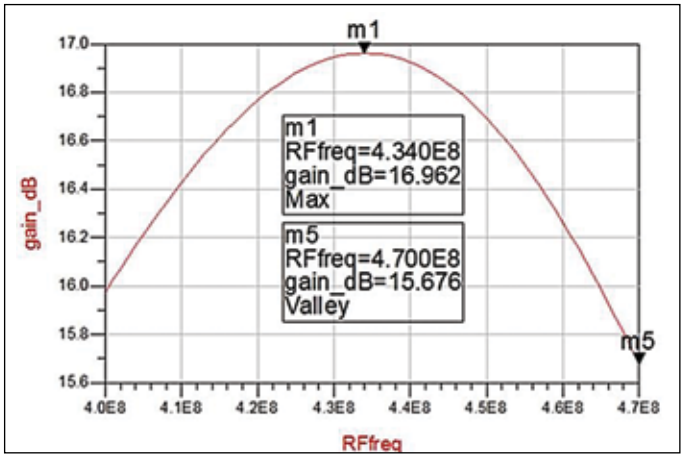

Figure 12 • Gain vs Frequency.

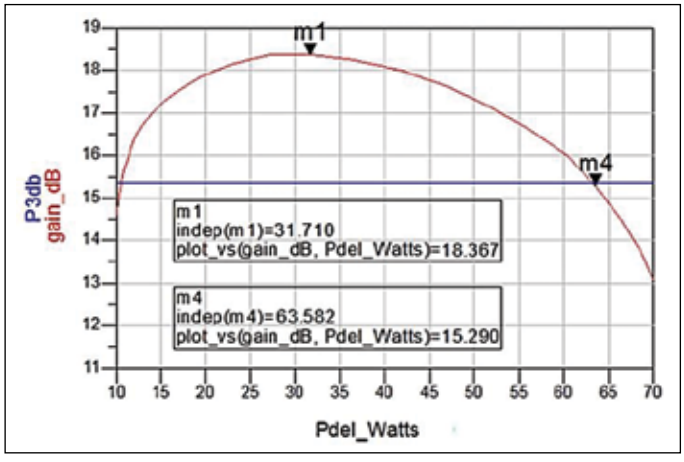

Figure 13 • Power vs Frequency.

The ZLot was then synthesized using lumped elements and microstrip lines.

Similarly the 1st stage has been matched at central frequency in order to get a good input return loss (IRL) along the band.

Finally all the stages were assembled and the final circuit with COB is hereafter displayed:

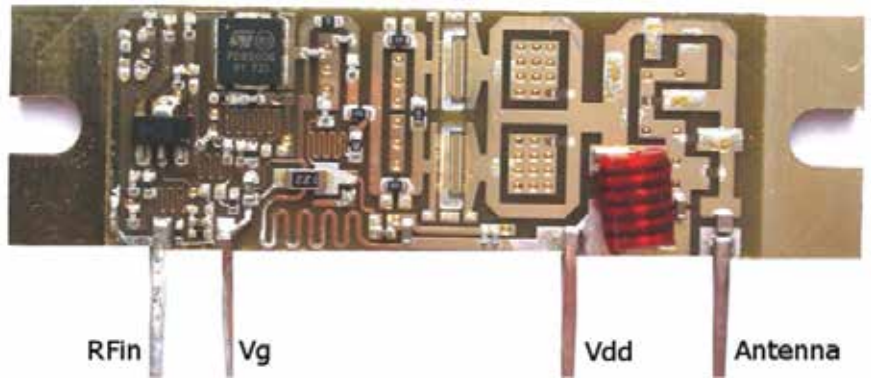

Figure 14 • COB module.

The prototype (Figure14) has been then measured in order to verify all the RF performances (see test-bench Figure 20).

On the RF bench the prototype has been optimized and in some part re-tuned. The measurements are hereafter presented:

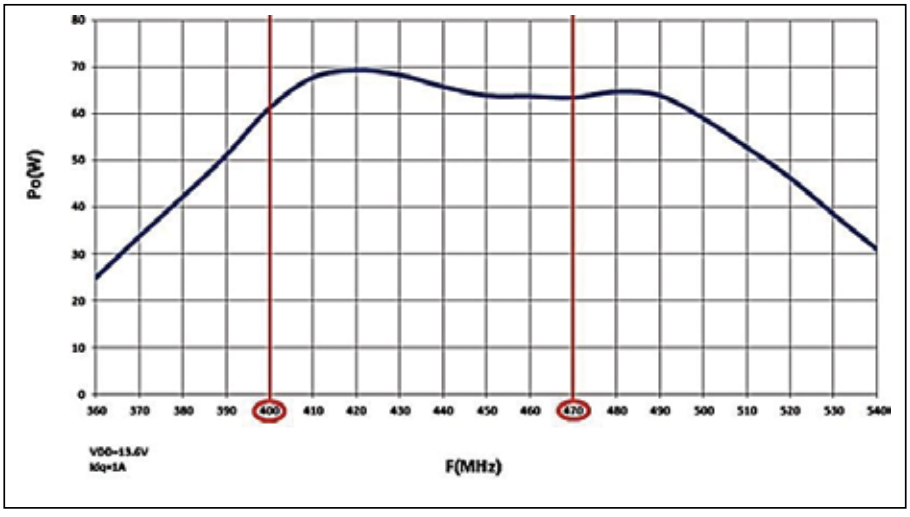

Figure 15 • Po vs frequency of COB.

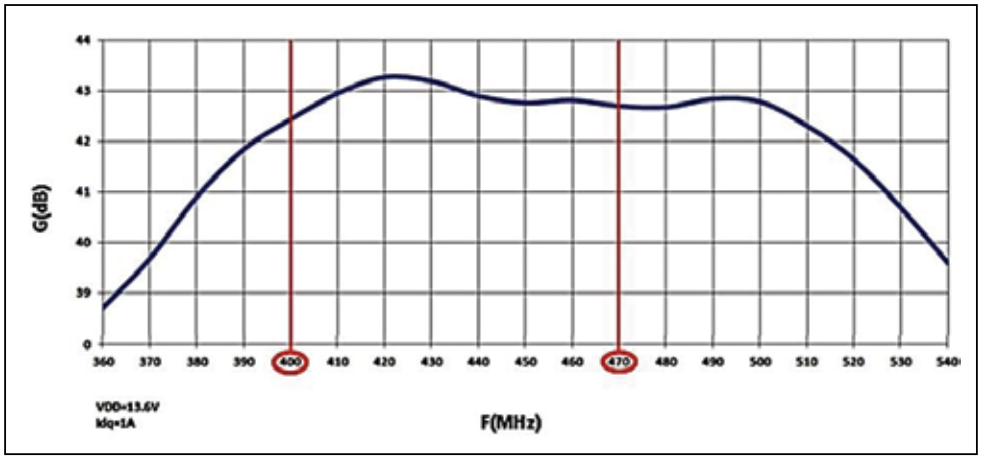

Figure 16 • Gain vs Frequency of COB.

In conclusion, the preliminary design done with COB has delivered better than expected results. This was possible thanks to the synergy between simulations and the RF bench re-works.

At this point, in order to verify if both parallel dice were working in a balanced way (i.e. if they carried half of the total power present in the output) a thermo analysis was performed.

A thermal map of the dice's surfaces could unveil hot spots and potential failures. Moreover it's a good way to check the solder joint between PCB and the area beneath the dice.

The thermal measurements (Figure 17) showed about 10 °C of difference between the two average temperatures, proving that both devices are working properly.

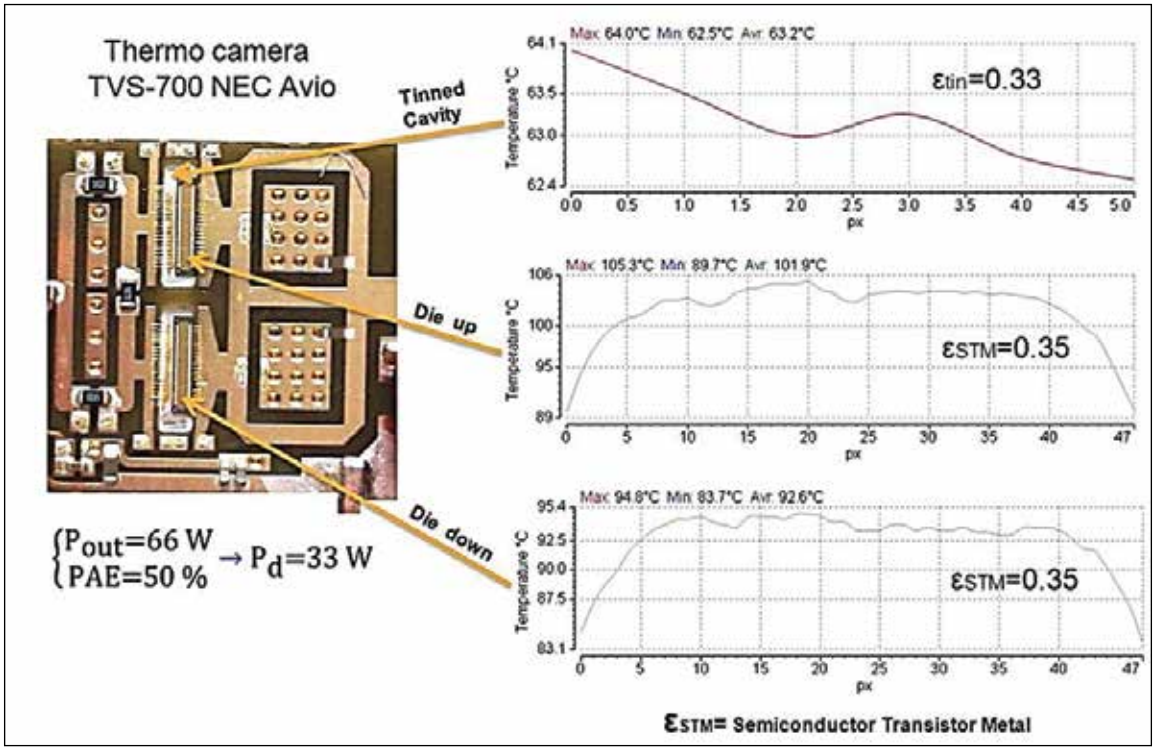

Figure 17 • Thermal map.

Design of the Discrete Modules

After the preliminary design made in COB we are now able to set up the cascade 1st and 2nd stage. Moreover, we have a better understanding of the power capabilities of the two dice. Now it's time to move on making the prototypes stated in Table 1.

For both projects we have used the same topology of PCB shown in Figure 18. Moreover, to test the amplifiers, we have developed a special test board and heat-sink (Figure 19). Their BOM is presented in Table 4.

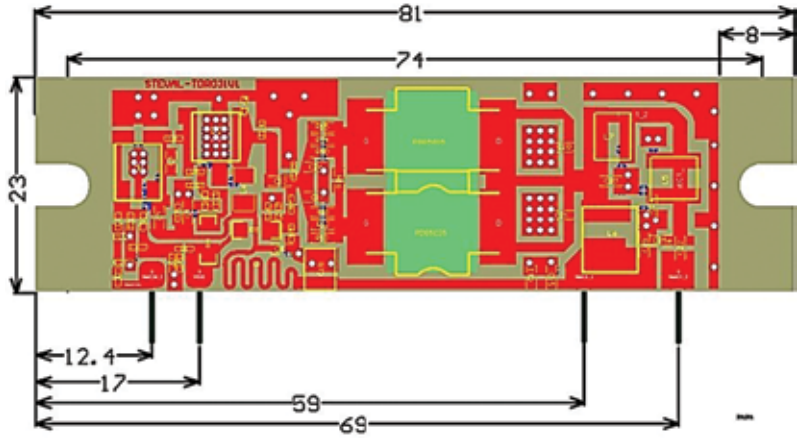

Figure 18 • PCB for modules.

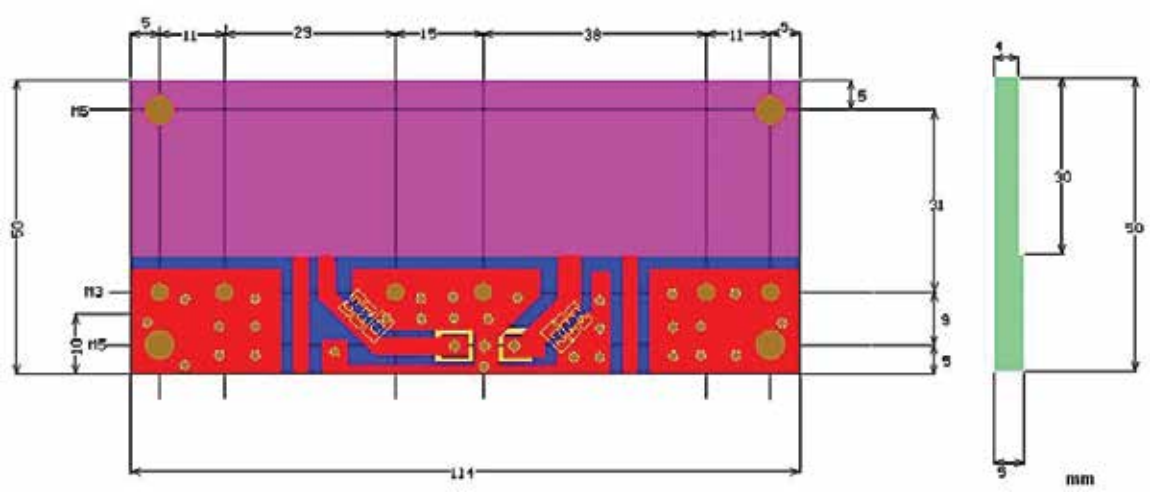

Figure 19 • Test board.

All the measures were done with test bench as shown in Figure 20.

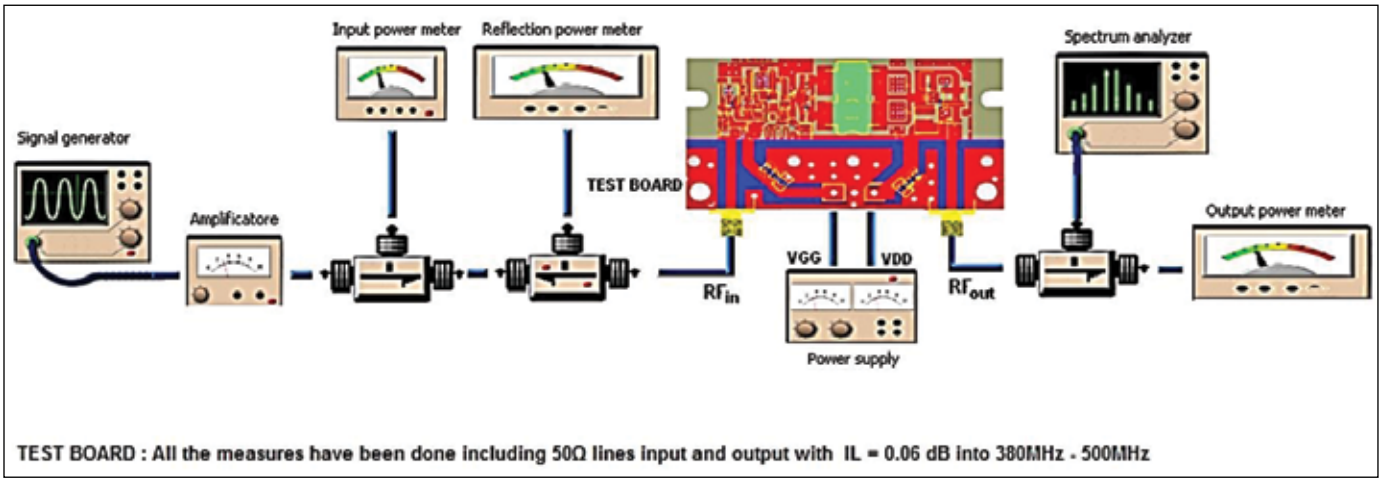

Figure 20 • Test bench.

STEVAL-TDR031V1

This design moved along the same lines previously adopted for the COB version.

No big changes concerning the 1st and the 2nd stage. All the activity was focused on searching for the optimum load impedance at central frequency.

The load was then used to optimize the RF behaviors along the frequency band.

The result of this work is presented in the following images.

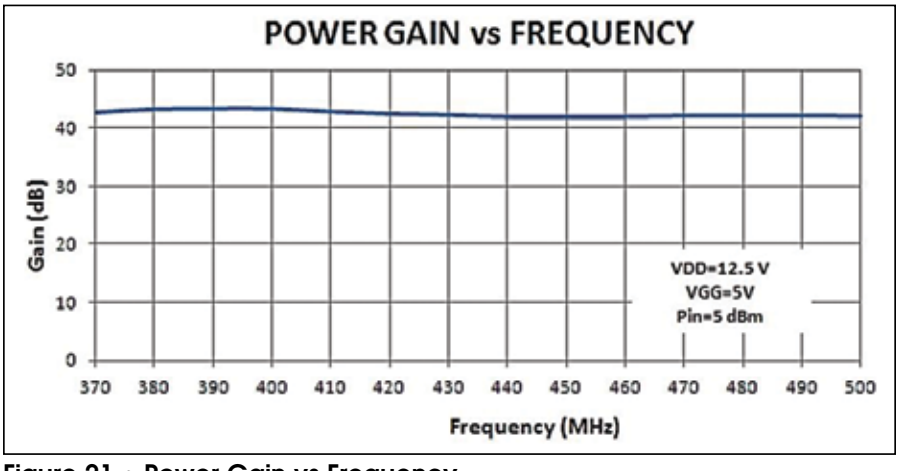

Figure 21 • Power Gain vs Frequency.

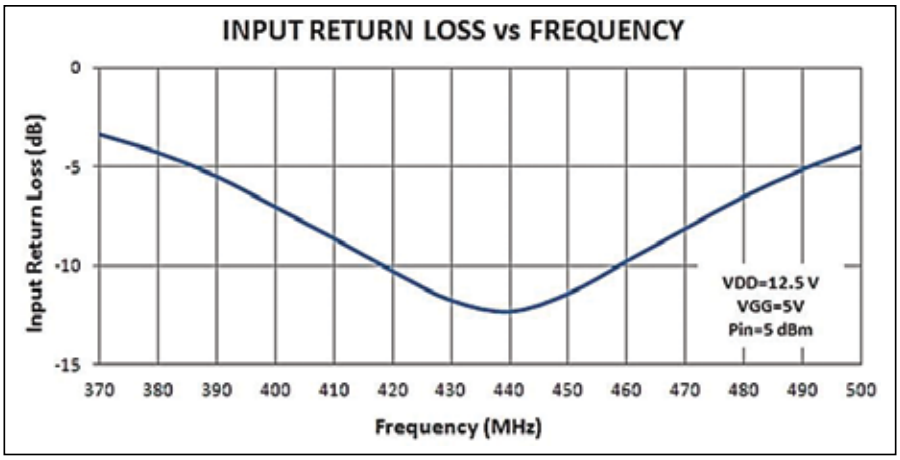

Figure 22 • IRL vs Frequency.

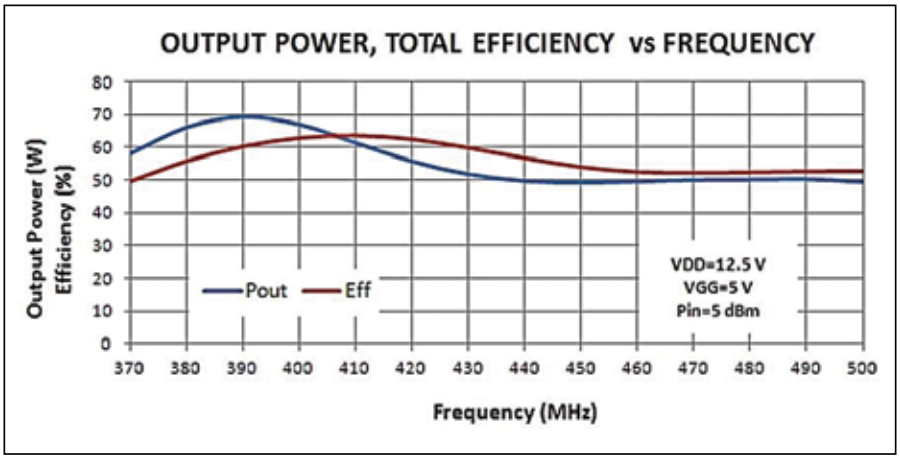

Figure 23 • Po, eff. Vs Frequency.

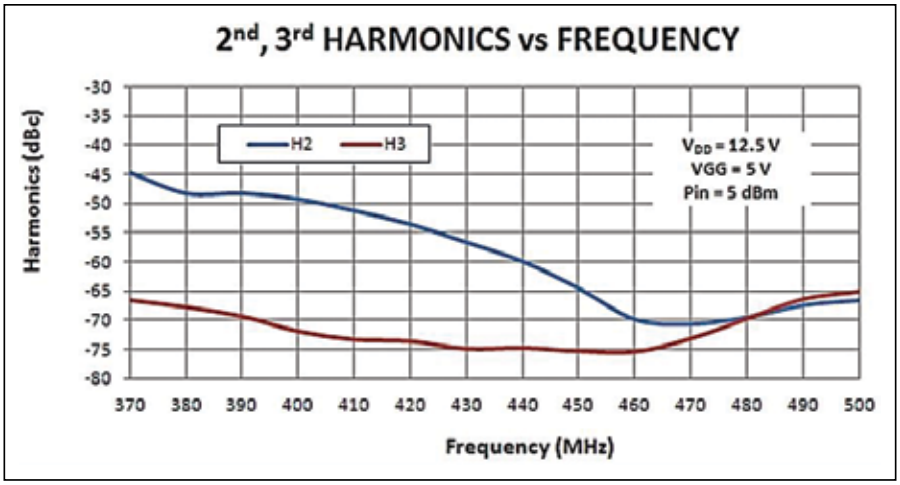

Figure 24 • Harmonics.

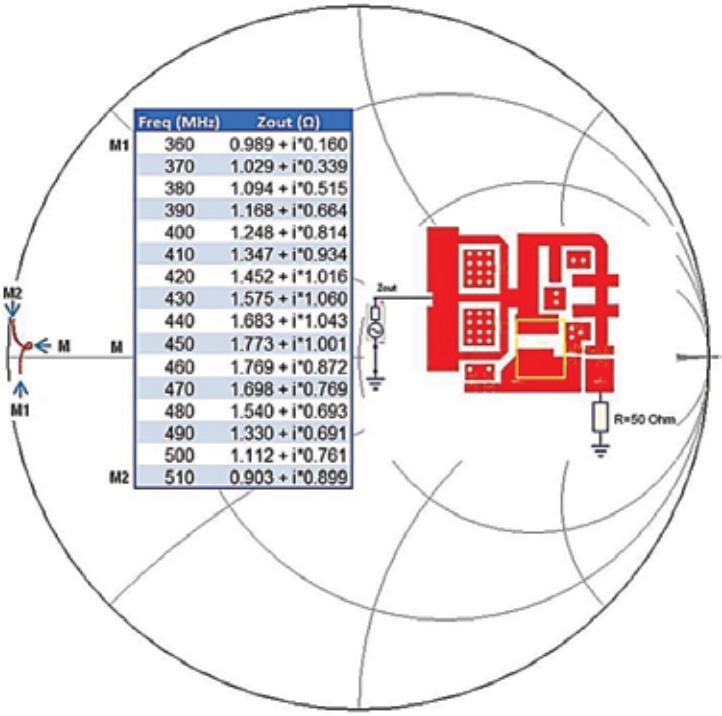

Figure 25 • Output impedance of STEVAL-TDR031V1

In Figure 25 we see the equivalent drains' impedances for the two PD85035S-E measured at the midpoint between the two drains. The small circle around the mark M (Figure 25) proves the achievement of broadband impedance.

The STEVAL-TDR031V1 is visible in Figure 26 while for the schematic and BOM refer to Figure 27 and Table 2.

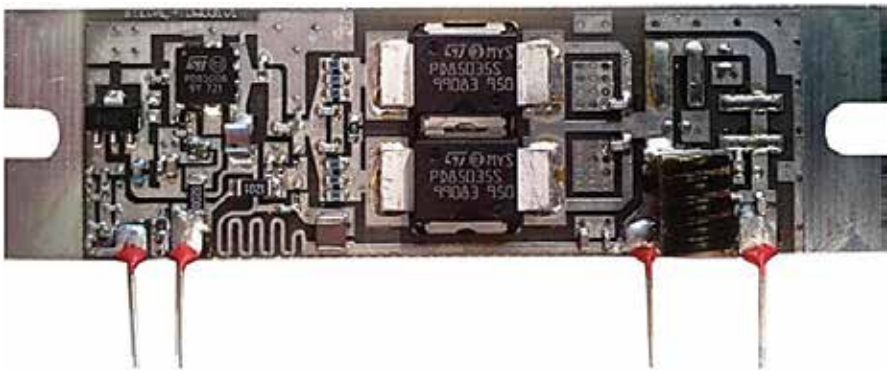

Figure 26 • STEVAL-TDR031V1.

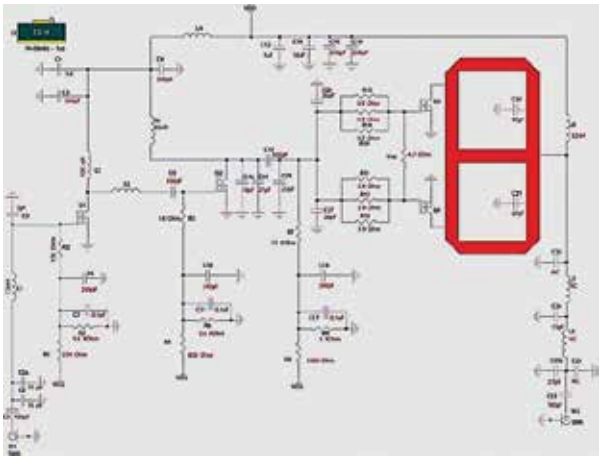

Figure 27 • Schematic of STEVAL-TDR031V1.

Designator	Manufacturer	Quantity	Value	Manufacturer Part Number	Footprint
C1, C9	Murata	2	100pF	GRM1555C1H101JA01	402
C2	Murata	1	16 pF	GJM1555C1H160GB01#	402
C2a	Murata	1	10 pF	GJM1555C1H100JZ01#	402
C3	Murata	1	5pF	GRM1555C1H5R0GA01#	402
C4	Murata	1	1uF	GRM188R61E105KA12#	603
C5, C6, C8, C10, C15, C16, C19	Murata	7	240pF	GRM1555C1H241JA01#	402
C7, C11, C17	Murata	3	0.1uF	GRM155C81E104KA12#	402
C12	Murata	1	1uF	GRM188B31E105KA75#	603
C13	Murata	2	100pF	GQM1885C1H101GB01#	603
C22	Murata	2	100pF	GQM2195C1H101JB01#	805
C14	Murata	1	27pF	GRM1555C1H270FA01#	402
C14a	Murata	1	18pF	GRM1555C1H180JZ01#	402
C18	Murata	1	10uF	GRM32ER71H106KA12#	1210
C20, C21	Murata	2	47pF	GQM1875C2E470GB12#	603
C24	Murata	1	15pF	GQM1875C2E150GB12#	603
C25a	Murata	1	2.7pF	GCM1885C2A2R7CB01#	603
C26, C27	Murata	2	36pF	GRM1555C1H360GA01#	603
C29	Murata	1	22pF	GRM1555C1H220FA01#	402
L1	Coilcraft	1	7.5nH	0402CS-7N5XJLW	402
L2	Coilcraft	1	100 nH	0603HP-R10X_LU	603
L3, L4	NA	2	NA	NA	402
L5	Coilcraft	1	10.2nH	0807SQ-10N_LC	Mini A
L6	Coilcraft	1	52nH	NA5778-AE	
L7	Coilcraft	1	3.7nH	GA3092-ALC	Mini A
La	Coilcraft	1	68nH	1008HQ-68NX_LC	402
Q1	STM	1	SOT89	PD84002	SOT89
Q2	STM	1	PowerFlat	PD85006L	PowerFlat
Q3, Q4	STM	2	PSO-10	PD85035S	PSO-10
R1	Vishay	1	220 Ohm	CRCW0402220RFKED	402
R2	Vishay	1	150 Ohm	CRCW0402150RFKED	402
R3, R6	Vishay	2	5.6 KOhm	CRCW04025K60FKED	402
R4	Vishay	1	820 Ohm	CRCW1206820RFKEA	1206
R5	Vishay	1	18 Ohm	CRCW040218R0FKED	402
R7	Vishay	1	15 KOhm	CRCW040215K0FKED	402
R8	Vishay	1	1200 Ohm	CRCW12061K20FKEA	1206
R9	Vishay	1	4,99 Kohm	CRCW04024K99FKED	402
R10, R11, R12, R13, R14, R15	KOA Speer	6	3.9 Ohm	RK73H1JTTD3R90F	603
R16	Vishay	1	4.7 Ohm	CRCW06034R70FKEA	603
Substrate			FR-4	20 mils 1oz copper	

Table 2 • BOM of STEVAL-TDR031V1.

STEVAL-TDR034V1

The final stage of this amplifier employs two PD85050S. Based on the latest low voltage LDMOS technology, these devices satisfy the increasing demand for power in the context of UHF mobile radios. In applications for digital communications, sometimes the linearity must be obtained with some dB of back-off from the power saturation. Using the PD85050S device model, some load-pull simulations were performed in order to get the optimum load impedance that allowed the max output power. The value has been then divided by 2 (parallel of two PD85050S) and considered as the starting point during the synthesis of the output network. The RF results and the impedance level measured at the drain level are shown in the below figures.

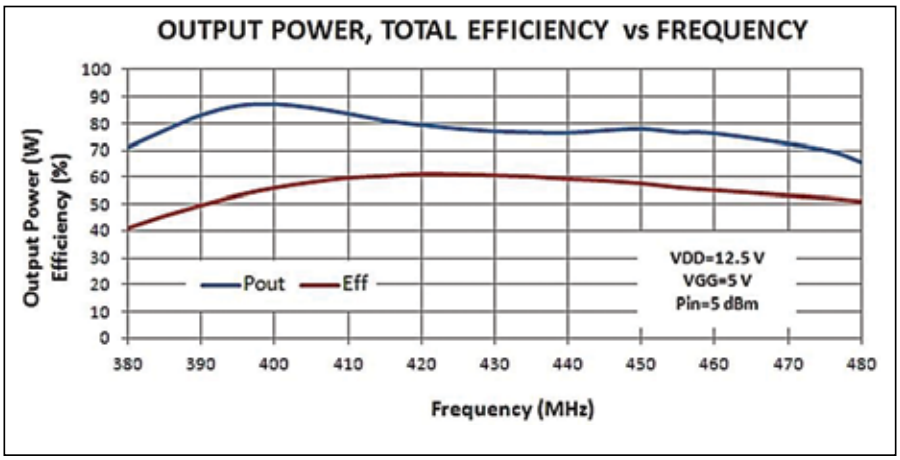

Figure 28 • Po, Eff. Vs Frequency.

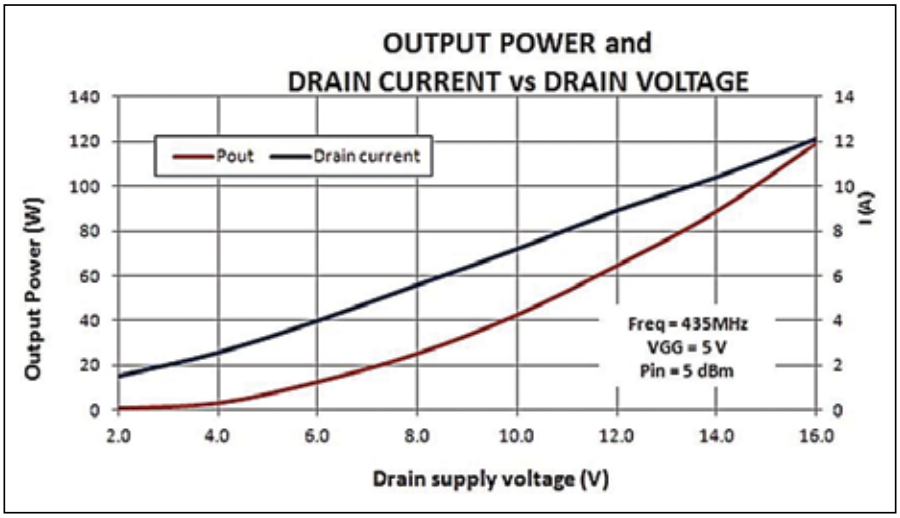

Figure 29 • Po, Id vs Voltage supply.

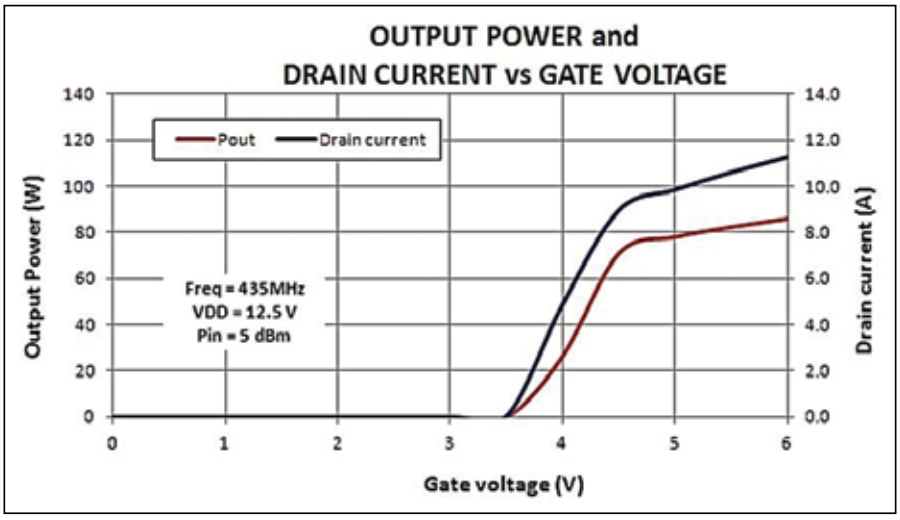

Figure 30 • Po, Id vs gate supply.

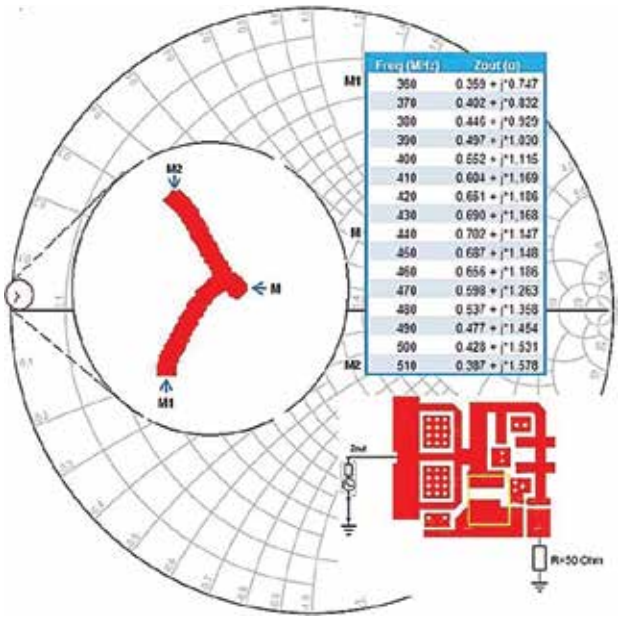

Figure 31 • Output impedance of STEVAL-TDR034V1.

The STEVAL-TDR034V1 is visible in Figure 32 while for the schematic and BOM refer to Figure 33 and in Table 3.

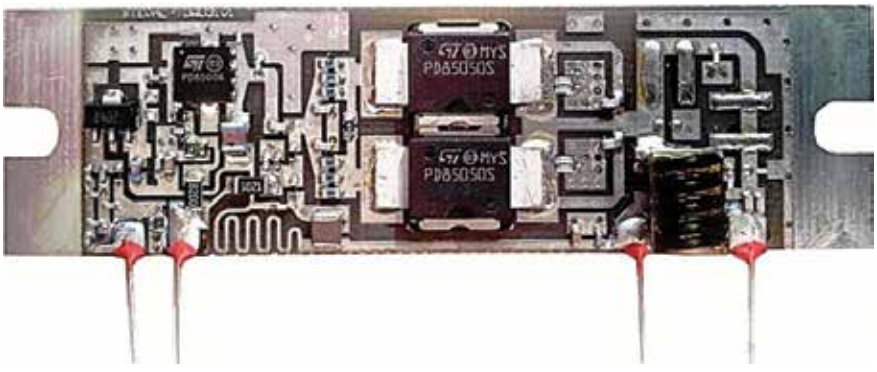

Figure 32 • STEVAL-TDR034V1.

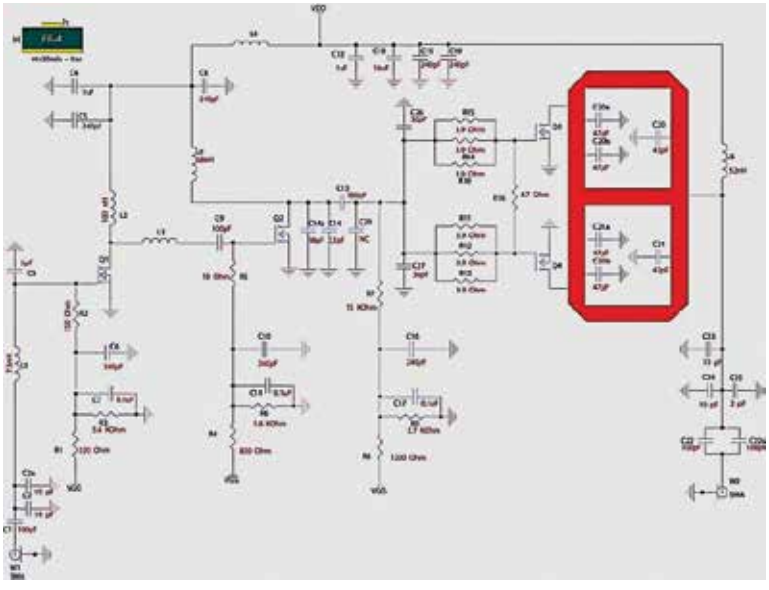

Figure 33 • Schematic of STEVAL-TDR034V1.

Designator	Manufacturer	Quantity	Value	Manufacturer Part Number	Footprint
C1, C9	Murata	2	100pF	GRM1555C1H101JA01	402
C2	Murata	1	16 pF	GJM1555C1H160GB01#	402
C2a	Murata	1	10 pF	GJM1555C1H100JZ01#	402
C3	Murata	1	5pF	GRM1555C1H5R0GA01#	402
C4	Murata	1	1uF	GRM188R61E105KA12#	603
C5, C6, C8, C10, C15, C16, C19	Murata	7	240pF	GRM1555C1H241JA01#	402
C7, C11, C17	Murata	3	0.1uF	GRM155C81E104KA12#	402
C12	Murata	1	1uF	GRM188B31E105KA75#	603
C13	Murata	1	100pF	GQM1885C1H101GB01#	603
C22, C22a	Murata	2	100pF	GQM2195C1H101JB01#	805
C14	Murata	1	27pF	GRM1555C1H270FA01#	402
C14a	Murata	1	18pF	GRM1555C1H180JZ01#	402
C18	Murata	1	10uF	GRM32ER71H106KA12#	1210
C20, C20a, C20b, C21,C21a, C21b	Murata	6	47pF	GQM1875C2E470GB12#	603
C23, C24	Murata	2	10pF	GQM1875C2E100JB12#	603
C25	Murata	1	2pF	GCM1885C2A2R0CB01#	603
C26, C27	Murata	2	36pF	GRM1555C1H360GA01#	603
C29	Murata	1	NC		
L1	Coilcraft	1	7.5nH	0402CS-7N5XJLW	402
L2	Coilcraft	1	100 nH	0603HP-R10X_LU	603
L6	Coilcraft	1	52nH	NA5778-AE	
La	Coilcraft	1	68nH	1008HQ-68NX_LC	402
Q1	STM	1	SOT89	PD84002	SOT89
Q2	STM	1	PowerFlat	PD85006L	PowerFlat
Q3, Q4	STM	2	PSO-10	PD85050S	PSO-10
R1	Vishay	1	220 Ohm	CRCW0402220RFKED	402
R2	Vishay	1	150 Ohm	CRCW0402150RFKED	402
R3, R6	Vishay	2	5.6 KOhm	CRCW04025K60FKED	402
R4	Vishay	1	820 Ohm	CRCW1206820RFKEA	1206
R5	Vishay	1	18 Ohm	CRCW040218R0FKED	402
R7	Vishay	1	15 KOhm	CRCW040215K0FKED	402
R8	Vishay	1	1200 Ohm	CRCW12061K20FKEA	1206
R9	Vishay	1	2,7 Kohm	CRCW04022K7CEED	402
R10, R11, R12, R13, R14, R15	KOA Speer	6	3.9 Ohm	RK73H1JTTD3R90F	603
R16	Vishay	1	4.7 Ohm	CRCW06034R70FKEA	603
Substrate			FR-4	20 mils 1oz copper	

Table 3 • BOM of STEVAL-TDR034V1.

Designator	Manufacturer	Quantity	Value	Manufacturer Part Number	Type
C1, C2		2	100µF		Tantalum
C3, C4	Murata	2	10µF	GRM42-6X7R225K25D52K	402
C5, C6	Murata	2	2.2uF	GRM42-6X5R106K25D539	603
Substrate			FR-4	60 mils 1oz copper	

Table 4 • BOM Test Board.

Conclusion

This article has described a design procedure and some practical solutions to build a multistage power amplifier. The intent was to show a low-cost and reliable way to design and produce customizable amplifiers.

The STEVAL-TDR031V1 and STEVAL-TDR034V1 were designed with plastic packaged LDMOS devices, resulting in amplifiers with a high moisture sensitivity level typically not achievable with similar modules using chip-on-board technology.

STMicroelectronics can provide all the LDMOS devices mentioned in this article, and if necessary, can also provide the technical support to revise the layout (gerbers) for system integration and/or the components for cost reduction (BOM) .

Standard design support includes: device models, PCB gerbers, BOM and demo board, for further information please visit www.st.com/rf.

References

1. Cripps, S. C., RF Power Amplifiers for Wireless Communications, Norwood, MA: Artech House, 1999.
2. Andrei Grebennikov, RF and Microwave Power Amplifier Design, McGraw Hill,2005.

About the Author:

Alfio Scuto was born in Acireale, Italy, in 1967. He received a Master's degree in Electronics Engineering with Microelectronics from the University of Catania, Italy, in 1998. In 1999, he joined STMicroelectronics and, for two years, worked in the RF power design center based in Montgomeryville, PA. Since then he has been involved in the device characterization of high-power high-frequency transistors, such as DMOS and LDMOS. He is currently working in STMicroelectronics in Catania (Italy) as a Senior RF Engineer supporting the product marketing group. For many years he has designed and developed RF power amplifiers to evaluate and verify product performance in reference to customer requirements.