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LNA With a Bypass Mode Improves Overload Resistance for Mobile TV

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This article is a case history describing the design choices and tradeoff considerations required to meet a particular set of customer specifications

Television (TV) stations broadcast in the very high frequency (VHF; 30-300 MHz) and ultra high frequency (UHF; 300-900 MHz) bands. Opposite to the small cell philosophy popularized by modern wireless telephone service, free-to-air TV broadcast is historically driven by the need to extend the area of coverage, as doing so will garner a larger audience. So, commercial TV transmissions utilize tall aerial towers and power level in the 10-50 kW range in order to maximize their radio horizon. In comparison, the transmit power of a cellular repeater is many magnitude orders lower at ~50 W.

Mobile TV allows the commuting public to watch TV programs on hand-held or portable devices [1]. The mobile TV functionality can be incorporated into notebook personal computers, Personal Digital Assistant (PDA), In-Car-Entertainment (ICE) system [2], and cellular handsets, etc. Technically, the mobile TV poses a unique problem in that the distance between the transmitter and receiver can change considerably as the user travels to different locations. Given that only miniature aerials (i.e., low gain aerials) can be embedded in these portable products, the TV receiver must understandably be designed with very high sensitivity to permit clear reception at the coverage fringes. Unfortunately, the large RF gain will result in overloading of the mixer and IF stages when the user moves into the proximity of high power TV transmitters. Once the signal waveform is distorted by an over-driven amplifier or a mixer, it cannot be corrected by simple filtering or signal processing.

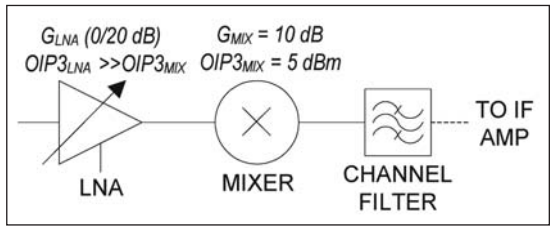

Figure 1 · Block diagram of receiver front-end with a variable-gain LNA stage. Mixer performance is reflective of consumer-grade TV receiver RFICs.

Input signal	LNA gain (dB)	Total gain (dB)	Total output IP3 (dBm)	Total input IP3 (dBm)
Weak	20	30	5	–25
Strong	0	10	5	–5

Table 1 · Gain and IP3 values for the receiver front-end in Figure 1.

Although it is technically possible to engineer higher overload tolerance in the mixer and IF stages, the required hardware will be too prohibitively expensive for this price-driven product category. Practical implementations of the mobile TV receiver almost universally rely on reducing the overall gain in the presence of strong signals as this is a far more cost effective solution to the overloading problem—hence the need for gain-controlled RF and intermediate frequency (IF) amplifier stages. The ability to vary RF gain greatly relaxes the linearity requirement in the mixer stage [3] and therefore allows low cost radio

Input shunt	Medium	Medium	Input match, selectivity*
LNA stage bypass	High	Highest	None
Reduce bias current	Low	Lowest	Linearity
*high impedance damping version only			

Table 2 · Cost-performance comparison of the various LNA gain control methods.

frequency integrated circuit (RFIC) with lesser linearity performance to be used for implementing the receiver. A cascade analysis of a receiver front-end with switchable LNA gain (Fig. 1 and Table 1) shows that the overall third order input intercept point (IIP3) can be improved by the same amount as the gain change. Hence the receiver that can alter its RF gain will have better large signal handling compared to one with a fixed gain.

The LNA gain can be varied automatically and without additional control circuit by making use of the wideband automatic gain control (AGC) function that is ubiquitous to contemporary broadcast receiver RFICs [4, 5]. Because the wideband AGC is derived from the part of the signal chain before the channel selecting filters, it is also able to respond to overload from adjacent channel transmissions.

A Survey of Common Topologies for LNA Gain Reduction

One widely adopted approach to reduce the RF gain is to shunt part of the signal to ground just before the LNA stage (Fig. 2a). This scheme owes its popularity to the minimal number of RF switching elements. However, it suffers from a major weakness in that the closed switch introduces a large impedance mismatch at the LNA input, and the consequential standing waves may affect other system parameters. To maximize the gain reduction, a variation of this technique connects the damping element to the high impedance side or "hot" end of the LNA parallel resonant network; this technique is popular in automotive sound and home TV broadcast receivers because they use variable tuning parallel resonant LC filters a.k.a. "pre-selectors." However, by shorting the tuned circuit, the pre-LNA RF selectivity is sacrificed for a larger gain control range [6].

An alternate approach bypasses the LNA stage with a pair of RF switches when the received signal is overloading the stages further down the receive signal chain; i.e., mixer or IF amplifiers. The non-amplified signal from the aerial is then directly routed to the down-converter RFIC (Fig. 2b). As long as the components in the alternate route (e.g., aerial, microstrip trace in the bypass path and the input to the down-converter RFIC) are designed with the same characteristics impedance (e.g., 75 Ω), no mismatch is introduced into the signal path. Nevertheless, using a pair of RF switches results in a higher circuit complexity than the other methods.

A third method reduces RF amplification by lowering the LNA device's quiescent current (Fig. 2c) and has seen wide adoption in LNA designs based on dual-gate MOSFET [7], cascode [8], differential pair of common emitter amplifier [3, 7] and quadrature pair [3]. These types of amplifiers are characterized by additional non-RF input terminals (e.g., G2 of the dual gate MOSFET and the base of the cascode's common base stage) that can be conveniently used for controlling the bias current. This method results in the lowest circuit complexity as no switching element is required, but suffers from progressively poorer linearity as the collector/drain current is reduced from the device normal DC operating point [9].

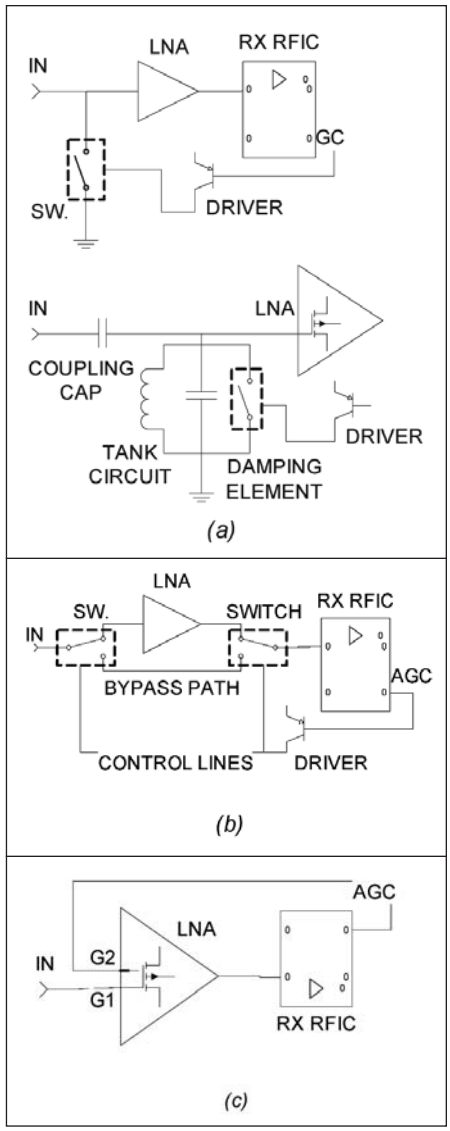

Figure 2 · Three common methods for RF gain control in consumer-grade broadcast receivers: (a) LNA input damping, (b) LNA bypass switching and (c) gate bias modulation in a dual gate MOSFET LNA. The LNA gain is automatically reduced based on feedback from the down-converter RFIC's AGC.

Parameter	Target	This work
LNA Gain (dB)	15 ~ 20	18.5 ~ 21
LNA noise figure (dB)	< 1.3	0.8 ~ 1.3
LNA IIP3 (dBm)	≥ 6	9.5 ~ 12.5
Bypass Loss (dB)	> –5	–3.8 ~ –4.5
bypass IIP3 (dBm)	≥ 20	> 20
LNA Current Id (mA)	< 200	30
Test frequency range: 47-870 MHz		

Table 3 · Comparison of customer's target requirements versus this design's measured results.

Application Background

The customer, a maker of consumer TVs, requested a reference design that must satisfy the RF specifications listed in Table 3. The intended application is LNA of a dual mode (analog/digital) mobile TV receiver in the 47-870 MHz range. In addition to the performance requirements, low component count and cost of implementation are also crucial to customer acceptance

Initially, existing MMICs from Avago Technologies' product portfolio, which consist of field effect transistors as both amplifying and switching elements (e.g., MGA-72563 or MGA-785T6), appeared to be the best candidates. A highly integrated monolithic solution such as one of these will result in the lowest cost, footprint and current consumption. After checking the devices' product specifications, we realized that these MMICs cannot fulfill the wide bandwidth and linearity requirements. Finally, we settled on a solution that combines a wideband, high linearity MMIC LNA (MGA-68563) with an external RF switch consisting of PIN diodes.

Component Selection and Circuit Design

This MGA-68563 MMIC is a single stage GaAs pHEMT amplifier with gate width of 800 microns (Fig. 3). The device gate is connected to an internal current mirror to compensate for process variations and to minimize the effects of threshold voltage variations. It utilizes lossy negative feedback for circuit stability and to flatten the frequency response to a 3 dB deviation from 0.1 to 1 GHz [10]. The MMIC is verified to be unconditionally stable as it has larger than unity Rollett stability factor values ($k \geq 1$) in the 0.1 to 4.0 GHz range.

As this MMIC was originally designed for single-frequency applications, its product specification recommended a simple input matching network consisting of one series inductor. Due to the previously described heavy internal feedback, no output matching is required as the output return loss is already good (ORL ≥ 10 dB) below 1 GHz. However, it is difficult to match the input over the 4-octave frequency range (47-870 MHz) using conventional LC networks. An RF transformer can match the input over the required bandwidth, but it was ruled out on cost and height reasons. So, instead of matching the device conventionally, the FET drain current (Ids) is varied above the 10 mA nominal value to optimize the input return loss (IRL). Although the required IRL (≥ 10 dB) is already met using a 20 mA Ids current, a final value of 30 mA was chosen because it allows more margin for the IRL to be degraded by the subsequent addition of the PIN diode switching circuit. The MMIC pin 4 controls the current flow through internal bias generator

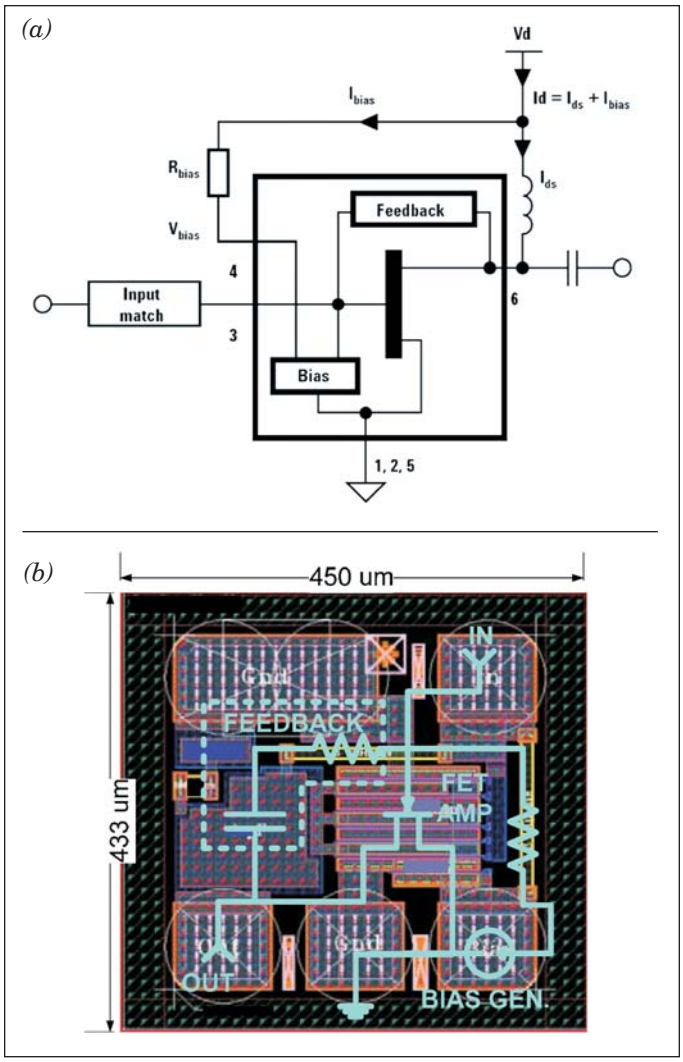

Figure 3 · MGA-68563 MMIC LNA (a) The simplified equivalent circuit where the MMIC on-chip components are shown enclosed by the thick-lined box while outside the box are the external components needed for input matching, bias control and drain supply decoupling. (b) The die layout with the functional components superimposed over it.

via an external resistor R1 (Figs. 3a, 5b) and therefore, redimensioning R1 conveniently changes Ids while the supply voltage Vd is fixed at 3.0 V. An incidental benefit that can be expected from the 300% increase in Ids is higher linearity.

The first design iteration required four PIN diodes to implement the switch by-passable LNA (Fig. 5a). This configuration is a fairly standard way to implement a double pole double throw (DPDT) switch using PIN diodes and is common in tower mounted LNAs, which must be bypassed during transmit. The circuit operates by turning on the upper pair of PIN diodes while the lower pair is zero

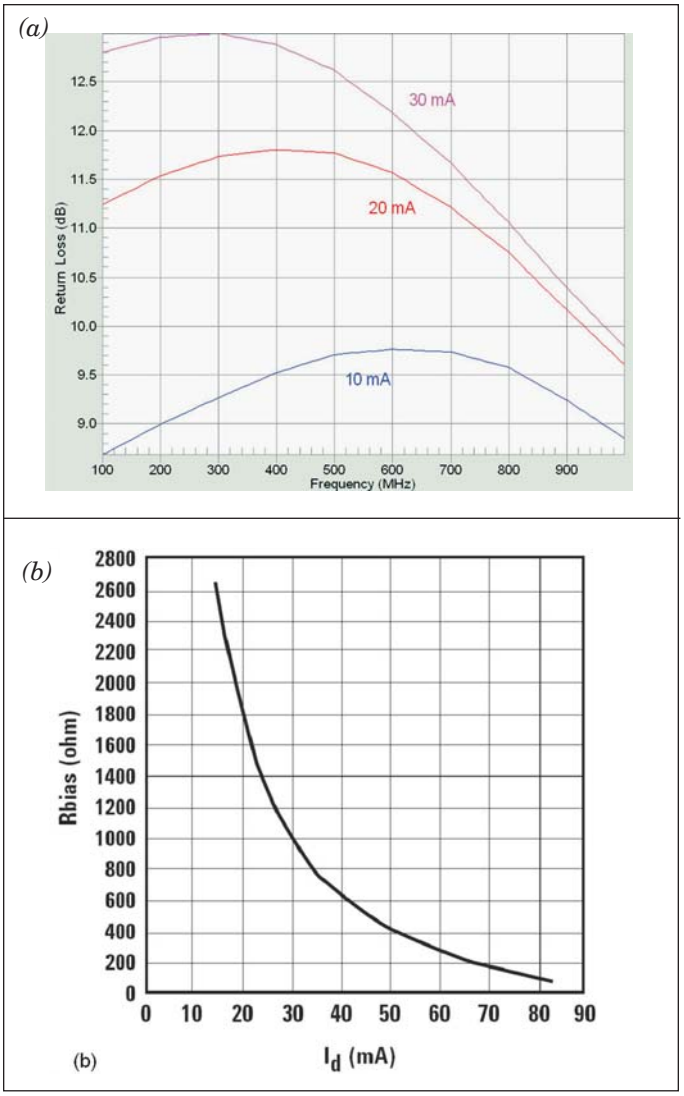

Figure 4 · (a) IRL vs. frequency as function of the FET drain current, Ids. IRL improves with higher Ids and so increasing Ids can obviate the need for input matching, and (b) The relationship between R1 (Rbias) and Ids.

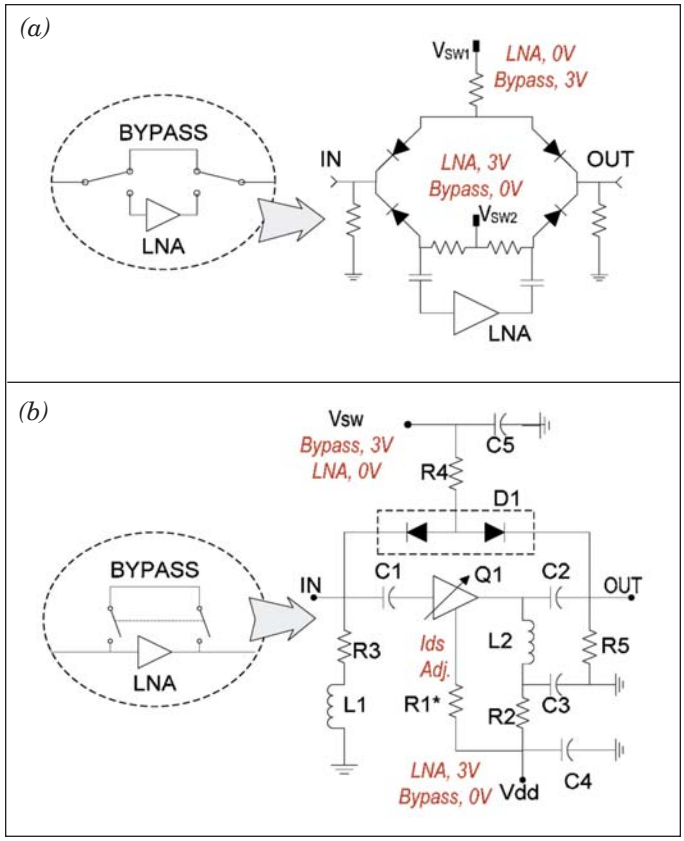

Figure 5 · Evolution of the switching circuit (a) initial four PIN diode design and (b) eventual design with reduced number of PIN diodes.

biased and vice-versa. During normal operation, only the lower PIN diode pair is turned on and so the RF signal is amplified by the LNA. When it is necessary to reduce RF gain, only the upper PIN diode pair is turned on in order to route the signal around the LNA (i.e., bypass mode). The resistors are required for regulating the PIN diodes' forward current and for isolating the RF signals from the logic control ports (VSW1 and VSW2). Despite meeting the customer's performance expectations, the component count raised a customer objection.

Following the customer feedback, a different switch circuit arrangement was devised to halve the previous design's number of PIN diodes. In the revised design as shown in Figure 5b, only the bypass path is connected or disconnected from the input and output ports by PIN diodes in a greatly simplified double pole single throw (DPST) arrangement.

Due to the absence of switching elements in LNA path, the LNA supply (Vdd) has to be switched off during the bypass mode in order to make use of the intrinsic isolation of the unbiased FET. A trade-off of this design is that the RL of the bypass path is poorer due to being shunted by the finite gate and drain impedances of the unbiased FET.

During normal LNA operation, the PIN diodes supply is turned off (V_{SW} = 0V) while the LNA supply is restored to 3V. However, the zero-biased PIN diodes have some parasitic capacitances that allow the higher frequencies to pass through. So, the LNA's gain and RL are compromised by the incomplete disconnection of the bypass path from the input and output ports.

L1 and L2 are ferrite beads inductors, and their function in the PIN diodes' and the MMIC's biasing networks is to present high impedances over the entire frequency range (Fig. 5b). Without L1's choking action, part of the input signal will be shunted to ground via R3's parallel-connected parasitic capacitance [11]. Measurement of a

Comp.	Value / part number
C1	1 nF
C2	47 pF
C3	1 nF
C4	1 µF
C5	1 nF
D1	Hsmp-3893/E
L1	Murata BLM18RK102SN
L2	Murata BLM18RK102SN
Q1	MGA-68563
R1	270 R
R2	4.7 R
R3	270 R
R4	270 R
R5	270 R

Table 4 · Value / part number of components associated with the circuit diagram in Figure 5b.

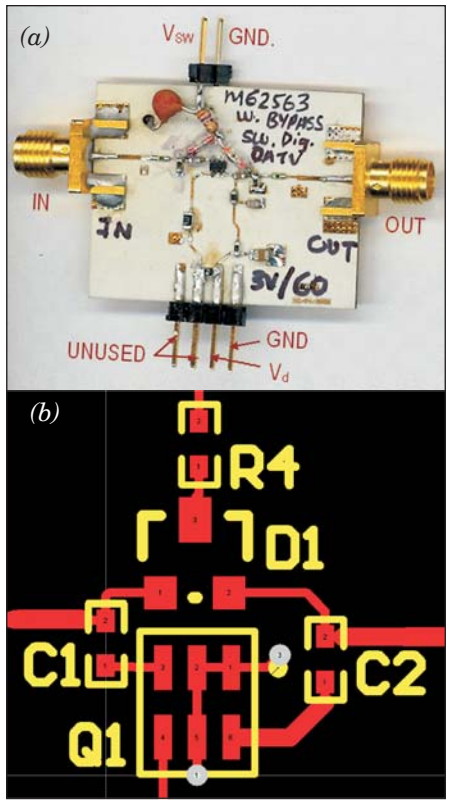

Figure 6 · (a) The "proof-of-concept" prototype; (b) the PCB layout revised to accommodate an SOT-23 surface mount PIN diode pair in the position D1.

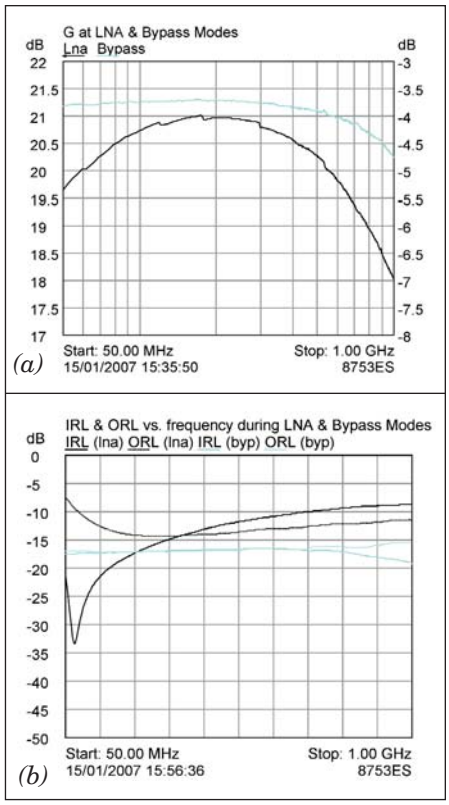

Figure 7 · Test results for both LNA and bypass modes of operation (a) gain vs. frequency and (b) input and output RL vs. frequency.

prototype without L1 provides experimental verification that the aforementioned signal loss is detrimental to LNA noise figure (Fig. 8). C3-C5 decouple RF signals from the DC supply lines and are dimensioned to be low reactance (Xc ≤ 5 Ω) at the lowest operating frequency. C1 and C2 provide DC blocking at the MMIC input and output. A small value is deliberately chosen for C2 in order to create a high pass response that can compensate for the MMIC's intrinsic gain roll-off at high frequencies. R1 and R2 control the MMIC supply current, and they are dimensioned for 30 mA at Vdd of 3V. R3-R5 limit the PIN diodes' forward bias to ~2.5 mA per diode at VSW of 3V.

Logically, it is possible to further simplify the circuit by using only one PIN diode in D1. However, there is no advantage to doing so as the diode pair occupies the same SOT-23 or SOT-323 package as a single PIN diode, and the price difference is also negligible. Additionally, the PIN diodes pair confers two important performance advantages: (a) the series connection halves the parasitic capacitance, and (b) as the even-order harmonics generated by the anti-series PIN diodes are out of phase, they will self-cancel [12].

Assembly of the Prototype

For a quick evaluation of the new design's RF performances, the "proof of concept" prototype was assembled on a printed circuit board (PCB) that has been previously designed for another non-bypassed LNA application [13]. The PCB is composed of micro-strip traces on 10 mil thick Rogers RO4350B dielectric material [14]. The PIN diodes and their associated biasing components were retrofitted to the existing PCB by directly soldering them to the leads/pads of the other components (Fig. 6a). Two pieces of 1N5719 axial-lead glass diodes [15] were used as the switching elements D1. These diodes will be eventually replaced by the SOT packaged PIN diode pair HSMP-3893/E [16] in a later PCB layout iteration (Fig. 6b).

Measurement Results and Discussion

The LNA's median gain is 19.8 dB with a 1.3 dB variation within the frequency range of interest (Fig. 7a). The frequency response is flattened by gently attenuating signals below 200 MHz using the high pass response imparted by an atypically small value of DC blocking capacitor C2. The gain roll-off at the upper frequency end is consistent with the MMIC characteristics and possibly with the negative feedback through the unbiased PIN diodes' parasitic capacitance.

The bypass mode has an attenuation of –3.8 to –4.5 dB over frequency (Fig. 7a). The bypass loss is mainly caused by the PIN diodes' parasitic series inductances. PCB dissipation, the FET terminal impedances and

R4's parasitic parallel capacitance also influence the bypass loss but to a smaller extent. However, no attempt was made to improve the present design's bypass loss as it is well within the customer-requested –5 dB specification limit.

In the bypass mode, both IRL and ORL are consistently good (better than –17 dB) in the specified frequency range. This parameter is primarily affected by how closely the unbiased FET gate and drain approximate open circuits. Both IRL and ORL fare slightly poorer during LNA operation with a worst case specification of –7 dB occurring at the output side on the lowest frequencies. The poor ORL below 70 MHz is caused by the small value capacitance in C2 and is accepted as a trade-off for a flatter frequency response.

Figure 8a compares the LNA noise figure with and without the ferrite bead inductor L1 in the prototype. It is obvious that the target noise figure specification (F ≤ 1.3 dB) cannot be met without L1. Comparing the two noise figure traces, it can be surmised that signal loss attributable to R3's parasitic capacitance is in the 0.3-0.6 dB range and, this has correspondingly pushed the noise figure up by the same amount. There is significantly more noise figure variation in the band with the inclusion of L1 than without (0.5 dB vs. 0.2 dB). However, no remedial action is planned as this is not a critical parameter. We hypothesize that this greater variation is caused by the ferrite bead's progressively reduced choking capability with increasing frequency, especially above the ~100 MHz self resonant frequency (SRF) that was estimated from the manufacturer-provided performance graphs [17].

The LNA's OIP3 is measured at several evenly spaced frequency points within the mobile TV band using a two-tone input power level of –20 dBm. The IIP3 is calculated by subtracting the measured gain from the OIP3 data. Within the measurement range, the OIP3 does not go lower than 30.3 dBm with a maximum 0.8 dB variation within the band (Fig. 8b). The linearity improvement of ~10 dB over the datasheet's nominal value (20 dBm) [10] can be attributed to this design's higher Ids (30 mA vs. 10 mA).

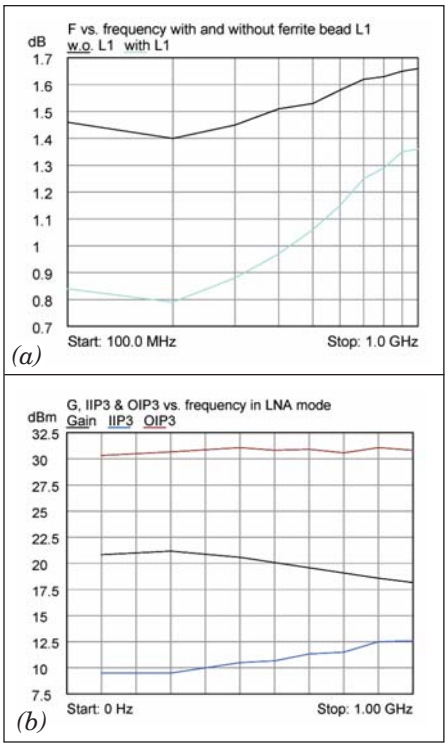

Figure 8 · LNA mode parameters: (a) noise figure vs. frequency when the prototype is tested with and without (w.o.) the L1 ferrite bead inductor and (b) IIP3 and OIP3 vs. frequency.

Conclusion

A wideband LNA with bypass function for mobile TV receivers requiring high overload tolerance was implemented using a combination of low noise pHEMT MMIC and PIN diodes. By increasing the FET Ids three times over the nominal value, the IRL can be improved to the extent of obviating the need for input matching. For cost and space saving reasons, the number of PIN diodes used to bypass the LNA stage was reduced from 4 to 2 by changing from the conventional DPDT switch arrangement to a DPST one. The design also satisfies all other target specifications set by the customer. A promising line of investigation for the future, especially if there is a customer request to further improve the LNA noise figure, is to replace the present ferrite bead inductor with higher SRF versions in order to lessen the noise figure variation with frequency.

Acknowledgement

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